2015

Investigation of Gate Dielectric Materials and Dielectric/Silicon Interfaces for Metal Oxide Semiconductor Devices

Lei Han
University of Kentucky, lei.han@uky.edu

STUDENT AGREEMENT:

I represent that my thesis or dissertation and abstract are my original work. Proper attribution has been given to all outside sources. I understand that I am solely responsible for obtaining any needed copyright permissions. I have obtained needed written permission statement(s) from the owner(s) of each third-party copyrighted matter to be included in my work, allowing electronic distribution (if such use is not permitted by the fair use doctrine) which will be submitted to UKnowledge as Additional File.

I hereby grant to The University of Kentucky and its agents the irrevocable, non-exclusive, and royalty-free license to archive and make accessible my work in whole or in part in all forms of media, now or hereafter known. I agree that the document mentioned above may be made available immediately for worldwide access unless an embargo applies.

I retain all other ownership rights to the copyright of my work. I also retain the right to use in future works (such as articles or books) all or part of my work. I understand that I am free to register the copyright to my work.

REVIEW, APPROVAL AND ACCEPTANCE

The document mentioned above has been reviewed and accepted by the student's advisor, on behalf of the advisory committee, and by the Director of Graduate Studies (DGS), on behalf of the program; we verify that this is the final, approved version of the student's thesis including all changes required by the advisory committee. The undersigned agree to abide by the statements above.

Lei Han, Student

Dr. Zhi David Chen, Major Professor

Dr. Cai-Cheng Lu, Director of Graduate Studies

INVESTIGATION OF GATE DIELECTRIC MATERIALS AND DIELECTRIC/SILICON INTERFACES FOR METAL OXIDE SEMICONDUCTOR DEVICES

DISSERTATION

A dissertation submitted in partial fulfillment of the
requirements for the degree of Doctor of Philosophy
in the College of Engineering
at the University of Kentucky
By

Lei Han

Lexington, Kentucky

Director: Dr. Zhi David Chen, Professor of Electrical Engineering Department

Lexington, Kentucky

2015

ABSTRACT OF DISSERTATION

INVESTIGATION OF GATE DIELECTRIC MATERIALS AND DIELECTRIC/SILICON INTERFACES FOR METAL OXIDE SEMICONDUCTOR DEVICES

The progress of the silicon-based *complementary-metal-oxide-semiconductor* (CMOS) technology is mainly contributed to the scaling of the individual component. After decades of development, the scaling trend is approaching to its limitation, and there is urgent needs for the innovations of the materials and structures of the MOS devices, in order to postpone the end of the scaling. Atomic layer deposition (ALD) provides precise control of the deposited thin film at the atomic scale, and has wide application not only in the MOS technology, but also in other nanostructures. In this dissertation, I study rapid thermal processing (RTP) treatment of thermally grown SiO_2, ALD growth of SiO_2, and ALD growth of high-k HfO_2 dielectric materials for gate oxides of MOS devices. Using a lateral heating treatment of SiO_2, the gate leakage current of SiO_2 based MOS capacitors was reduced by 4 order of magnitude, and the underlying mechanism was studied. Ultrathin SiO_2 films were grown by ALD, and the electrical properties of the films and the SiO_2/Si interface were extensively studied. High quality HfO_2 films were grown using ALD on a chemical oxide. The dependence of interfacial quality on the thickness of the chemical oxide was studied. Finally I studied growth of HfO_2 on two innovative interfacial layers, an interfacial layer grown by in-situ ALD ozone/water cycle exposure and an interfacial layer of etched thermal and RTP SiO_2. The effectiveness of growth of high-quality HfO_2 using the two interfacial layers are comparable to that of the chemical oxide. The interfacial properties are studied in details using XPS and ellipsometry.

KEYWORDS: Gate Leakage Current, Atomic Layer Deposition, Silicon Oxide, High-k Dielectric Material, Interfacial Layer

Lei Han

April 10, 2015

INVESTIGATION OF GATE DIELECTRIC MATERIALS AND DIELECTRIC/SILICON INTERFACES FOR METAL OXIDE SEMICONDUCTOR DEVICES

By

Lei Han

Zhi David Chen

Director of Dissertation

Cai-cheng Lu

Director of Graduate Studies

April 10, 2015

This dissertation is dedicated to my beloved family:

My father Shoucai Han

My mother Qiaoling Hao

My husband Qingquan Zhao

Acknowledgements

First and foremost, I would like to thank my advisor, Dr. Zhi Chen. This dissertation would not have been possible without his dedication of ideas, time, instructions, and funding. His enthusiasm for semiconductor device research as well as his precise insights in work have been incentive for me all through my Ph.D. studies. What I learned from him both in research and in real life would be a precious treasure which I would always benefit from in my future life.

Gratitude will go to my committee members, Dr. J. Todd Hastings, Dr. Vijay P. Singh and Dr. Fuqian Yang, for their time and suggestions. The valuable discussion and comments I received from them in my annual reviews and qualify exam greatly improved my Ph.D. research. I would also like to thank Dr. Chi-Sing Man for serving as the outside examiner for my Final Doctoral Examination.

I gratefully acknowledge all the members whom I worked with in Dr. Chen's group, Dr, Shibin Li, Dr. Chi Lu, Dr. Ibrahim Yucedag, Ms. Yichun Wang, Mr. Bojie Chen, and Mr. Xiaowei Zhang. The work and spare time we shared together have always been a source of diverse opinions as well as friendship. I am especially grateful for Yichun Wang. Her guidance for me after I joined this group has been greatly enlightening and helpful.

Special thanks also go to Dr. Charles May, Brian Wajdyk, and Jacob Hempel for always being ready to help at the Center for Nanoscale Science and Technology at the University of Kentucky.

Last but not least, I would like to dedicate my gratitude to my family. To my parents, who raised me up with pure love, and have always been supportive to me without any hesitation. I also thank my husband, Qingquan, who went through even the tough time in my Ph.D. pursuit together with me, having patience and giving me encouragement. With encouragement of my family, all my efforts are worthwhile.

Table of Contents

List of Tables

List of Figures

Chapter 1 Introduction

1.1 Scaling of the integrated circuit

The tremendous development of the integrated circuit (IC) technology in the past decades has laid a foundation for the overwhelming modern computer technology. Since the switching and amplifying functions of the traditional vacuum tubes and relays were realized by semiconductor-based transistors, the discrete components were replaced by an integrated circuit chip containing huge number of semiconductor devices. The implementation of the complementary metal-oxide-semiconductor (CMOS) technology promoted the functions of the integrated circuit, as well as a reduced static power consumption, and has become the mainstream technology in integrated circuits.

The development of the integrated circuit during the past decades has been driven by the scaling of the metal-oxide-semiconductor field effect transistor (MOSFET). The dimensions of the individual device in the integrated circuit have been markedly shrinking, increasing both the density and the performance of the integrated circuit. The scaling trend of the integrated circuit was summarized and predicted by the so-called Moore's law, indicating that the number of transistors that can be placed inexpensively on a dense integrated circuit doubles approximately every 18 months[1]. Since 1965, Moore's law has been successfully leading the progress of the semiconductor industry. The transistor counts in generations of microprocessors are plotted in figure 1.1. The logarithmic vertical scale of the plot indicates that the transistor counts have been exponentially increasing in each generation.

The average half-pitch, which means one half the average of the distance between metal lines in a generation of dynamic random-access memory (DRAM), is commonly used to define the technology node of microprocessors manufactured during the same time period. In 2014, Intel announced their 15-core Xeon Ivey Bridge-EX microprocessors built using the 22 nm technology, which contains 4.3 billion transistors. The first processor built with the 14 nm technology is the Intel Core M processor. At the beginning of this year, the 5th generation Intel Core processor was released, which is also built with the 14 nm technology, and 1.3 billion transistors are integrated. In the 2015 International Solid-State Circuits Conference (ISSCC) held in February, multiple leading companies including Intel, Samsung, etc. announced their progress in the 10 nm technology.

The increase of the integrated circuit density is desirable for apparent reasons: more devices could be integrated in the same area, enlarging the memory capacity and the functional capability. Additionally, the integrated devices are fabricated using photolithography, so the cost of individual device could be exponentially reduced by the large-scale integration. Integrated circuit meets a variety of technical requirements, including the circuit speed, the static (off-state) power consumption, and the ranges of the power supply and output voltages[2]. The most critical requirement differs according to the application areas of integrated circuits. For high performance logic circuits, such as that used in microprocessors, high speed is the prime goal, while for low power circuits, such as those used in cellphones, low static power consumption is the prime goal. The functional

performances of the integrated circuits also benefit from the diminishing of the dimensions of the MOSFETs.

The speed of high performance logic circuits is dependent on the drive current, which is the source-drain saturation current of the MOSFET. The improved performance of integrated circuits can be seen from the effect of the scaling on the drive current. The saturation current $I_{D,sat}$ of the MOSFET can be written as the following equation[3, 4]:

$$I_{D,sat} = \frac{W}{L}\mu C_{ox}\frac{(V_G - V_T)^2}{2} \tag{1.1}$$

where W and L are the width and length of the MOSFET channel, μ is the channel carrier effective mobility, C_{ox} is the gate oxide capacitance density, V_G is the gate voltage, and V_T is the threshold voltage. Reduction of channel length L, increase of channel carrier effective mobility μ and gate oxide capacitance density C_{ox}, will result in an increased $I_{D,sat}$. Adam Brand in *Applied Materials Inc.* summarized the scaling trend of the gate length since 1970s, the plot is cited here as the figure 1.2[5]. In spite of the exponentially increased transistor counts in the microprocessor and the continuously shrinked technology node, the redution of the gate length of the conventional planar MOSFETs has stopped since 2006, when it reached 35nm. The further scaling of the gate length requires innovations of device materials and structures, and the scaling concept is not only the dimensional shrinking any more, but the so-called “equivalent scaling”. The innovations of the device materials and sturctures will be illustrated in section 1.3.

The gate oxide capacitor could be modeled as a parallel plate capacitor, so the gate oxide capacitance density C_{ox} is defined as:

$$C_{ox} = \frac{k\varepsilon_0}{t_{ox}} \tag{1.2}$$

Where k is the dielectric constant of the gate oxide, ε_0 is the vacuum permittivity (8.85×10^{-12} F/m), and t_{ox} is the gate oxide thickness. Increase of the dielectric constant and reduction of the gate oxide thickness will result in an increased C_{ox}.

The success of integrated circuits could be largely attributed to the success of amorphous, thermally grown silicon dioxide (SiO_2) as the gate oxide for Si-based MOSFET. The appealing properties making SiO_2 an ideal gate oxide include: (1) sufficient dielectric constant (~3.9); (2) large band gap (～9eV) and suffcient band offsets with Si at both conduction and valence bands; (3) perfect Si-SiO_2 interface with interface trap density ~10^{10} $eV^{-1}cm^{-2}$; (4) good dielectric strength with breakdown electrical field >10 MV/cm; (5) thermal stability with Si even at high temperature; (6) good insulating strength for boron peneration from the p^+ poly-Si gate; (7) ease to thermally grow high quality SiO_2 on Si substrate at a low cost. These properties enabled Si to dominated the semiconductor industry for decades among other semiconductor materials, such as Ge, GaAs, InP, etc. The material properties of SiO_2 are summarized in table 1.1.

Reducing the thickness of the thermally grown SiO_2 in the Si-based MOSFET had been an effective way to increase the gate oxide capacitance density C_{ox} and the drive current $I_{D,sat}$,

until the thickness of the SiO_2 was reduced to ~3 nm with the 180 nm technology node[6]. At this oxide thickness range, the gate leakage current mechanism is mainly the direct tunneling, in which the current exponentially increases with the decrease of the gate oxide thickness[7]. Plus, the insulation of the boron penetration from the p^+ poly-Si gate is no longer effective[8, 9]. Struggling with these problems, the thickness of the SiO_2 was shrinked to 1.3 nm, when the effect of the further increased C_{ox} to the drive current $I_{D,sat}$ will be canceled out by the degradation of the channel carrier mobility[2, 10, 11]. The gate leakage current became unacceptable, resulting in extra power consumption, degradation of reliablility, peneration of impurity, and eventually malfunction of the MOSFET.

In order to keep up with the scaling trend predicted by the Moore's law, alternative gate oxide materials with dielectric constants higher than that of SiO_2 (high-k materials) were desired. The high-k gate oxide can be physically thick to reduce the direct tunneling current, and electrically thin to provide sufficient gate oxide capacitance density. The electrical thickness of the high-k gate oxide is evaluated using the concept "equivalent oxide thickness" (EOT), which means the thickness of the SiO_2 film needed to provide the same gate oxide capacitance density as the high-k oxide film. Referring to equation 1.2,

$$\frac{k_{SiO_2}\varepsilon_0}{EOT} = \frac{k_{high-k}\varepsilon_0}{t_{high-k}}$$

And

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} t_{high-k} \tag{1.3}$$

As reported in the international technology roadmap for semiconductors (ITRS, 2013 edition), the state of the art EOT of the logic high performance transistors is 0.8 nm, and it is predicted to be scaled down to ~0.4 nm in 2028[12]. The ITRS predictions of the EOT and the gate length are plotted in figure 1.3[12].

1.2 High dielectric constant (high-k) materials

Many dielectric materials have dielectric constants (k values) larger than that of SiO_2 (~3.9), ranging from Si_3N_4 (k~7) to $SrTiO_3$ (k~2000). Table 1.2 lists selected high-k dielectric materials and their approximate dielectric constants[13, 14]. A comprehensive summary of the high-k dielectrics and their properties is reported by O Engström, etc.[15].

In order to get high gate oxide capacitance, high dielectric constant is desired. However, high dielectric constant is not the only condition for a high-k dielectric material to be a successful substitute for SiO_2 in MOSFET. Some key requirements that a high-k dielectric material needs to meet in order to be an alternative gate oxide in CMOS technology are discussed below:

(1) Sufficient dielectric constant

Since the production cost of the semiconductor industry would be tremendously increased by the implementation of an innovative high-k material into the existing CMOS process flow, the dielectric constant should be large enough to support the performance improvement of microprocessors for several generations. Al_2O_3 has appealing properties

comparing to other high-k dielectric materials, such as large band gap, large conduction band and valence band offsets with Si, thermal stability with Si even at high temperature necessary for CMOS fabrication, good interfacial quality, etc.[16-20]. However, the dielectric constant of Al_2O_3 is only ~9, which limits its capability of increasing the drive current. Al_2O_3 is commonly used in memory application due to the low requirement of the circuit speed [21-24].

The actual dielectric constant of a high-k dielectric thin film varies according to the deposition techniques, the deposition parameters, and the ratio of the components in the material. O. Buiu etc. studied the relation between the dielectric constant of HfO_2 film and the Hf concentration, and reported that even for the same Hf concentration, the dielectric constant would be modified by the preparation method and properties of the interfacial layer between the HfO_2 film and the Si surface[25, 26].

(2) Band gap and band alignment to Si

Sufficient band gap of the high-k dielectric material is necessary, in order to reduce the gate leakage current. Robertson explored the relation between the band gap and the dielectric constant, and reported that in general, the band gap is in inverse proportion to the dielectric constant. This indicates materials with high dielectric constants usually have small band gaps, which would increase the gate leakage current[13, 27]. Figure 1.4 plots the band gap versus the dielectric constant for selected high-k materials.

Besides band gap, conduction band and valence band offsets of high-k dielectric materials with Si is another issue that needs to be considered in selection of proper gate oxide. The barrier height affects the gate tunneling current, either Fowler-Nordheim tunneling current or direct tunneling current, at an exponential rate[28-30]. Additionally, small barrier height would increase the Schottky thermionic emission, which is harmful to the channel carrier mobility of the MOSFET. Robertson calculated the conduction band and valence band offsets of a variety of high-k materials with Si[2, 27], there are also other published results verifying and supplementing Robertson's calculation[31, 32]. The band alignments of selected materials are drawn in figure 1.5. Among the high-k materials in this figure, HfO_2 and ZrO_2 have large band gaps and band offsets, making them ideal candidates to replace SiO_2 in semiconductor industry.

(3) Thermal stability in contact with Si

High temperature process is necessary in the CMOS technology, such as the dopant activation process. The desired thermal stability of high-k dielectric materials concerns the crystallization at high temperature, the formation of silicate, the growth of SiO_2 interfacial layer, etc.

Crystallization of high-k dielectric materials at high temperature must be avoided, because crystallization forms additional conduction path for gate leakage current. Preparation methods of the high-k materials affect the crystallization temperature. HfO_2 grown by molecular beam epitaxy (MBE) was reported to crystallize at 450°C[26, 33], while HfO_2

grown by sputtering of Hf in O_2 atmosphere was reported to crystallize at 700°C[2]. By optimizing the growth parameters and the gate technology, HfO_2 was successfully annealed at 1000°C without degrading the electrical properties of the device [34-36].

At high temperature, possible formation of metal-Si-oxide silicate at the high-k/Si or SiO_2 interface should also be avoided because it might create additional conduction path for gate leakage current and introduce short between source and drain. It was reported that HfO_2/Si interface is stable without formation of silicate, while ZrO_2/Si interface is not stable[37, 38], causing compatibility problem with poly-Si gate. This is the reason that HfO_2 has been chosen over ZrO_2 in CMOS technology. It is needed to clarify that some silicates are also high-k dielectric materials, and their properties have been explored [39-42]. The formations and structures of the high-k silicates are different from the thermal stability concern discussed here.

A SiO_2-like interfacial layer exists between high-k gate oxide and Si, improving the interfacial quality. However, the regrowth of the interfacial layer during the high temperature process must be strictly controlled in order not to increase the EOT of the gate oxide stack. It was explained through ternary phase diagrams that Ta_2O_5 and TiO_2 are not stable to SiO_2 formation [2, 43, 44], which limits their applications in CMOS technology. HfO_2 and ZrO_2 are well known of easy O_2 penetration, so O_2 must be get rid of from the atmosphere of the high temperature process.

(4) Low interface trap density

The defects at the gate oxide/Si interface enhance the carrier scattering effect in the channel of transistors, degrading the carrier mobility. The best gate oxide/Si interface available in semiconductor industry is the thermal SiO_2/Si interface, the midgap interface trap density of which is ~$2\times10^{10}cm^{-2}$. The interface trap densities of high-k dielectric materials are all higher than that of SiO_2. The high-k dielectric materials usually have a flatband voltage (V_{FB}) shift from the theoretical value (work function difference between the semiconductor substrate and the gate), which might be partially attributed to the large amount of interface traps. Thus, the interfacial quality must be evaluated before applying a high-k dielectric material into the CMOS technology.

HfO_2 satisfies most of the requirements and made itself an outstanding candidate among all the high-k dielectric materials. The material properties of HfO_2 are compared with those of SiO_2 in table 1.1. HfO_2 was firstly applied into manufacturing of integrated circuits in 2007 by Intel and IBM in their 45 nm technology, and has successfully supported generations of microprocessors since then. Referring to the 2013 edition of the international technology roadmap for semiconductors (ITRS), the gate length of the HfO_2-based high performance logic transistor has been scaled down to 20 nm, and the EOT has been scaled down to 0.8 nm[12].

Various technologies can be used to grow HfO_2, such as MBE[26, 33], sputtering of Hf in O_2 atmosphere[45], electron-beam evaporation[46], re-oxidation using rapid thermal

annealing (RTA)[47], etc. Among these technologies, atomic layer deposition (ALD) provides atomic-level control of the film thickness, uniformity and stoichiometry on large areas, due to its self-limiting reaction. The ALD will be extensively discussed in section 1.4.

1.3 Recent innovations for further scaling

The aggressive scaling of transistors has reduced EOT of gate oxide to < 1 nm, and it is expected to be 0.41 nm by 2028. The gate length is also expected to be simultaneously scaled down from 20 nm to 5.1 nm[12]. The traditional way of diminishing the physical dimensions of transistors cannot support the aggressive scaling any more, innovative materials and device structures are desired, in order to keep up with the scaling steps predicted by Moore's law. The scaling realized by the innovations is called as the "equivalent scaling" to distinguish from the traditional scaling. Generally speaking, the architecture of transistors are switching from planar design to vertical design.

In the fully depleted (FD) silicon-on-insulator (SOI) MOSFETs, an ultrathin layer of insulator is placed on top of Si substrate, which is named as the buried oxide (BOX). An ultrathin layer of Si is placed between the BOX and the gate oxide, and it acts as the channel between source and drain. The cross sectional view of the FD-SOI MOSFETs is shown in figure 1.6. While the sharply increasing doping level of the channel creates scaling barrier for the traditional planar MOSFETs, there is no need to dope the channel of the FD-SOI MOSFETs due to its thinness. The electrical control of the FD-SOI MOSFETs is

intrinsically improved, enabling better performance. Additionally, the short channel effect and the source-drain leakage current are effectively reduced by the BOX. Using the FD-SOI MOSFETs, the scaling of the gate length could be pushed forward[48-50].

The FinFETs, which are vertical double-gate MOSFETs, were firstly developed by Chenming Hu etc. at the University of California, Berkeley[51-54]. The conductive channel is a thin wall with the "fin" shape wrapped by gate material, enabling good electrical control of the carriers from more than one direction (as shown in figure 1.7 (a)). The device is considered as vertical because two gates locate vertically on the two sides of the channel. The channel length is decided by the thickness of the gates. Using this design, the source-drain leakage current of the transistor is dramatically reduced, and the short channel effect is alleviated. Based on the FinFETs, multi-gate technologies have been developed by leading semiconductor companies. The structure of the Tri-gate transistors built by Intel is shown in figure 1.7 (b), where multiple fins are connected together. The Tri-gate transistors have been applied in Intel's products since the commercialization of the 22 nm technology (2011), and are considered to be the promising architecture for future scaling.

The ultimate electrical control of the conductive channel is expected to be realized by the gate-all-around (nanowire) transistors. The fundamental idea of the gate-all-around transistors is similar to that of the multi-gate transistors, except that the conductive channel is thoroughly surrounded by the gate material. The cross sectional views of the conductive

channels of the double-gate FinFETs, Tri-gate transistors and gate-all-around transistors are drawn together in figure 1.8 to compare. The conductive channel material is a bunch of nanowires, including Si nanowires and III-V nanowires[55-57]. The outstanding controllability of the conductive channel is expected to introduce tremendous improvement of the performance, and maximize the density of the integrated circuits.

Besides innovative architectures of transistors, materials with carrier mobility higher than that of Si are implemented into the integrated circuits in order to increase the drive current. Strained Si was firstly used by Intel in their 90 nm technology[58]. Germanium (Ge) and III-V materials have appealing mobility and are becoming desirable channel materials in up-to-date transistors. According to ITRS, the semiconductor industry is optimistic about InGaAs for *n*-channel and Ge for *p*-channel[12].

1.4 Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) has been an important technique in semiconductor processing that allows for atomic level control of thin film deposition. The invention of ALD concept can be traced back to 1960s with the name “molecular layering”, while in 1970s it was renamed as “atomic layer epitaxy” (ALE), and in 2000 it was finally renamed as “ALD”[59]. Although a number of applications have been demonstrated in ALD history such as preparations of epitaxial compound semiconductors and III-V compounds in 1980s[60], ALD was not widely applied until mid-1990s to grow the dielectric materials. The development of silicon-based semiconductor devices and integrated circuits motivated

and facilitated the exploration of ALD technique. The implementation of plasma broadened the material category that can be deposited using ALD (plasma-enhanced ALD, PEALD). Besides microelectronics, ALD has also been applied in a large variety of disciplines including magnetic recording heads, optics, protective coatings, and micro-electromechanical systems (MEMS)[60].

In principle, an ALD process refers to a sequential treatment of a surface containing a finite number of reactive sites, resulting in self-limiting reaction. The reactive species are saturated and the thin films are deposited with precise thickness control at the angstrom level. In an ideal circumstance with complete exposure and purge in each step, surfaces can only absorb precursor molecules (gases, volatile liquids or solids) until all reactive sites are saturated, prohibiting any further reactions. Due to the nature of self-limiting reaction, ALD has huge advantages over other thin film techniques, especially when pursuing film conformity on large size substrates, or on high aspect ratio structures[61]. Although the film thickness is affected by the size of precursor molecules, as well as the number of adsorption sites on surface, the thickness is mainly determined by the number of reaction cycles involved. In addition, since reactants are supplied separately and each step is pushed to completion, ALD process requires less need of reactant flux homogeneity than chemical vapor deposition (CVD) techniques. The ALD mechanism greatly expands the diversity of precursors and improves the tolerance towards small changes in experimental conditions such as temperature and precursor flow rate[60]. The effectiveness of ALD on substrates with complex structures also broadens its application.

One of the most important applications of ALD is to deposit high quality HfO_2, the mainstream dielectric material in microelectronic industry. A variety of organic precursors could be used, including hafnium tetrachloride ($HfCl_4$)[62], amino-type precursors such as tetrakis(ethylmethylamino)hafnium (TEMAH)[63] and tetrakis(diethylamino)hafnium (TDMAH)[64], cyclopentadienyl-type precursors such as $Cp_2Hf(CH_3)_{2[65]}$, etc. H_2O or O_3 can be used as the oxidant[66]. The deposition using $HfCl_4$ has been reported to be dependent on the surface preparation[67], while the dependence is remarkably alleviated with TEMAH and TDMAH[68-70]. Additionally, the products of the $HfCl_4$ and H_2O based ALD process include HCl, which is corrosive and harmful to the environment. Thus, the amino-type precursors are preferable. In figure 1.9, the chemical mechanism of the TDMAH and H_2O based ALD process is demonstrated.

1.5 Outline of the dissertation

The dissertation is devoted to the investigation of the gate dielectric materials and the dielectric/silicon interfaces in the Metal-Oxide-Semiconductor (MOS) structure, in order to improve the electrical properties of the MOS devices in the actual integrated circuits, as well as broaden the application of the gate dielectric materials on the nanostructures and reduce the industrial fabrication cost. Three goals have been achieved in the dissertation. Firstly, the electrical property of the widely used thermal SiO_2 has been tremendously improved using an innovative thermal treatment. Secondly, ultrathin SiO_2 film has been deposited by ALD, the material and electrical properties of the film and the SiO_2/Si interface have been extensively evaluated. Thirdly, the desirable interface conditions for ALD of high quality HfO_2 have been discussed, and two original interfacial layers have

been developed; the properties of the interfacial layers have been comprehensively studied, and the potential benefits to the industry have been proposed.

In Chapter 2, fabrication of the MOS capacitor is illustrated in details. In addition, a wet etching process for patterning of the metal gate for the MOS capacitor is developed and evaluated. Comparison will be made between the MOS capacitors fabricated using the lift-off process and the wet etching process, and the advantages of the wet etching process will be demonstrated.

In Chapter 3, an innovative lateral heating treatment is developed using the rapid thermal process (RTP). After this treatment, the gate leakage current of the ultrathin SiO_2 based MOS capacitors was reduced by 4-5 orders of magnitude. The underlying correlation between the gate leakage current reduction and the material structure change will be explored in depth.

In Chapter 4, the deposition of thin SiO_2 films using ALD is discussed. The growth linearity, the electrical and material properties of the thin films, and the SiO_2/Si interfacial quality were characterized by the multi-angle spectroscopic ellipsometry and the multi-frequency capacitance density-voltage (C-V) measurement.

In Chapter 5, the ALD growth of high quality HfO_2 on chemical oxide interfacial layer is covered. The chemical oxides grown at various temperatures in different time duration were studied using the multi-angle spectroscopic ellipsometry. The dependence of the interfacial quality on the thickness of the chemical oxide will be discussed.

In Chapter 6, the preparation of an in-situ formed hydrophilic interfacial layer is illustrated. The interfacial layer was grown by ozone and H_2O exposure in the ALD chamber. The material properties of the interfacial layer were studied by the multi-angle spectroscopic ellipsometry and the X-ray Photoelectron Spectrometer (XPS). The effectiveness of the interfacial layer for the growth of the high quality HfO_2 will be compared to that of the chemical oxide.

In Chapter 7, an innovative interfacial layer for ALD of high quality HfO_2 is prepared by controllable etching of thermal and RTP SiO_2. The etching speeds of the oxides in diluted hydrofluoric acid (HF) solution were monitored by the multi-angle spectroscopic ellipsometry. The effectiveness of the interfacial layer was investigated by the electrical measurement of the MOS capacitors, and the chemical oxide interfacial layer was used as a reference.

In Chapter 8, the presented work in the dissertation is summarized, and the future research directions are proposed.

Table 1.1. Material properties of SiO_2 and HfO_2.

Material Properties	**SiO_2**	**HfO_2**
Dielectric constant	~3.9	~20
Band gap (eV)	9	6
Conduction band offset with Si (eV)	3.5	1.5
Valence band offset with Si (eV)	4.4	3.4
Density (g/cm^3)	2.27	9.68
Bulk refractive index	1.46	2.2
Melting point (°C)	1600	2758
Interface trap density ($cm^{-2}eV^{-1}$)	$\sim10^{10}$	$\sim10^{11}$

Table 1.2. Selected high-k dielectric materials and their dielectric constants[13, 14].

Material	Si_3N_4	Al_2O_3	Y_2O_3	La_2O_3	Ta_2O_5	TiO_2
k	~7	~9	~15	~30	~22	~80
Material	HfO_2	ZrO_2	$ZrSiO_4$	$HfSiO_4$	$SrTiO_3$	
k	~25	~25	~13	~11	~2000	

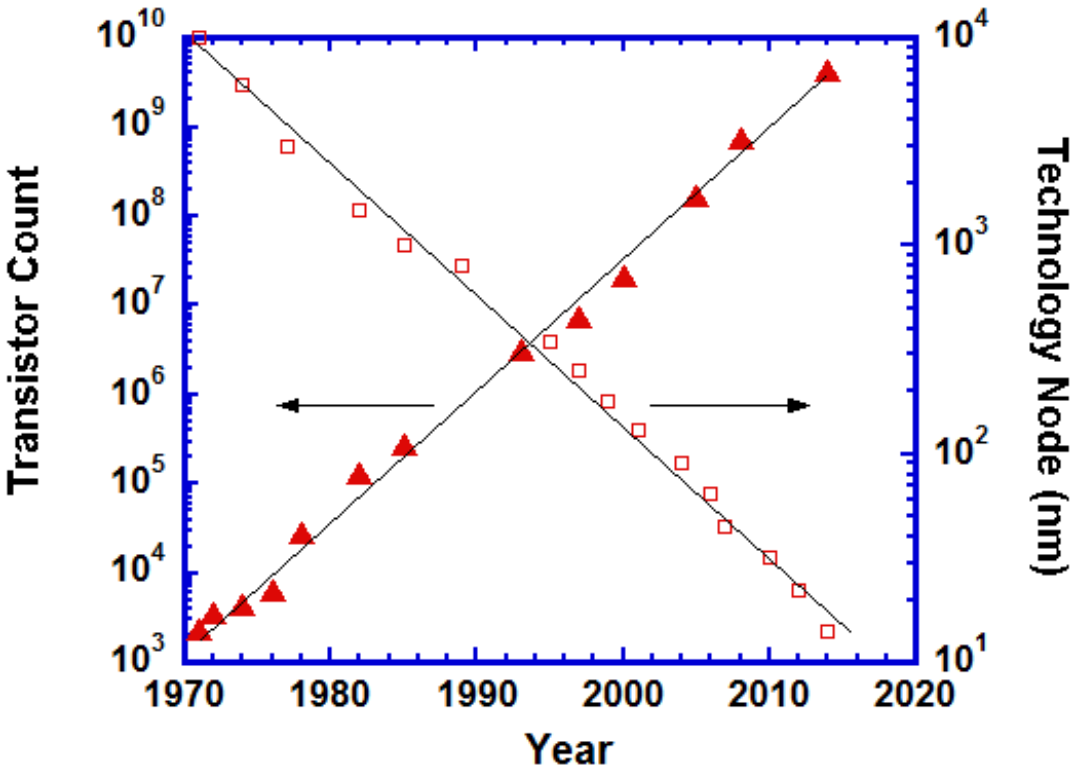


Figure 1.1. Number of transistors in state-of-the-art microprocessors from 1971 to 2014.

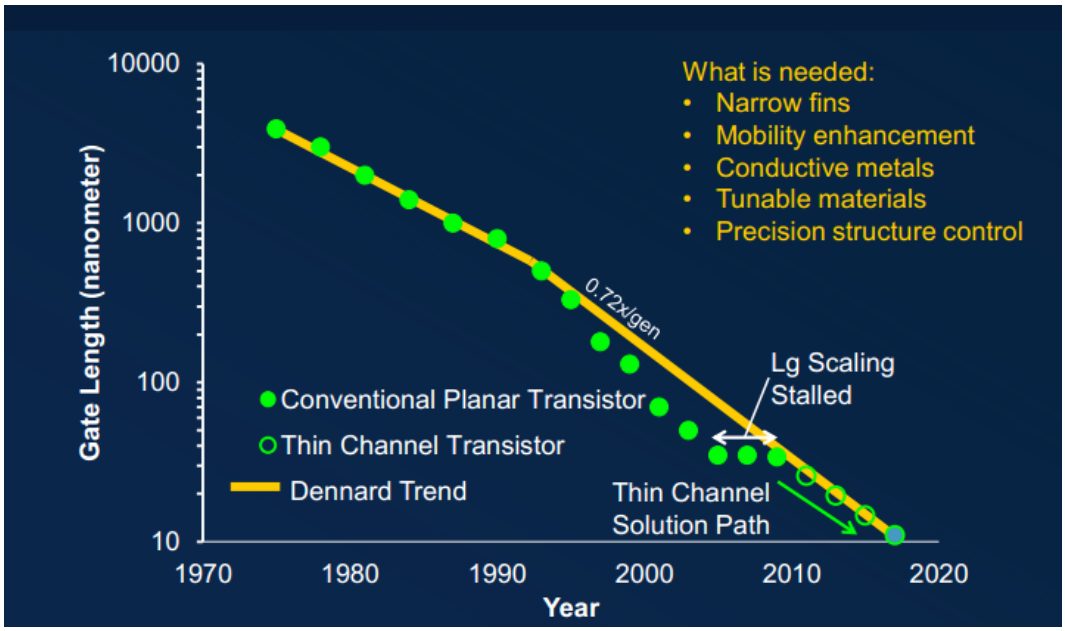
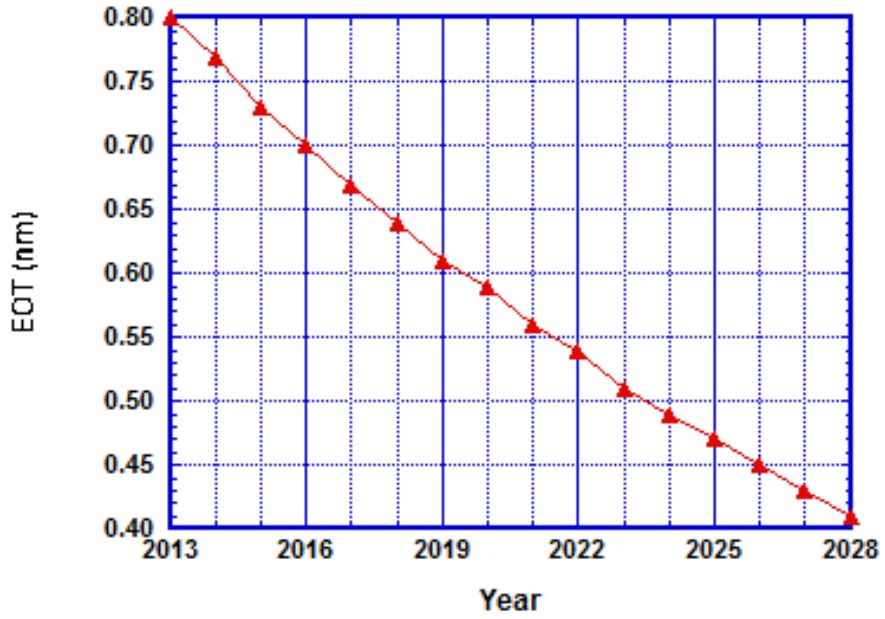
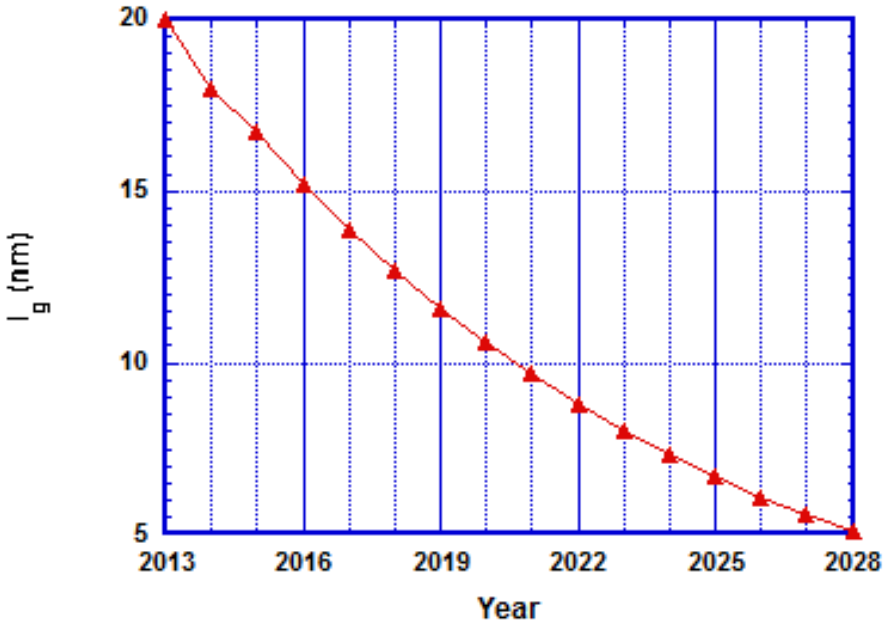


Figure 1.2. The scaling trend of the transistor gate length[5].



(a)



(b)

Figure 1.3. Prediction of the scaling of (a) transistor EOT and (b) transistor gate length by ITRS 2013 edition[12].

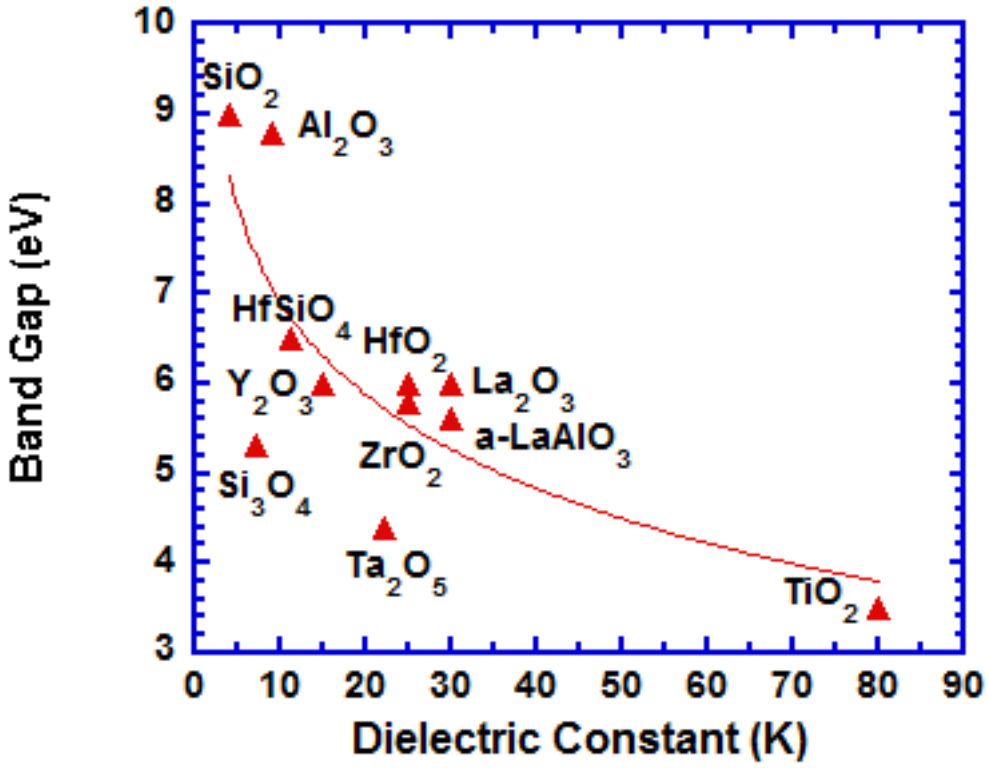


Figure 1.4. Band gap versus dielectric constant for various high-k materials[13].

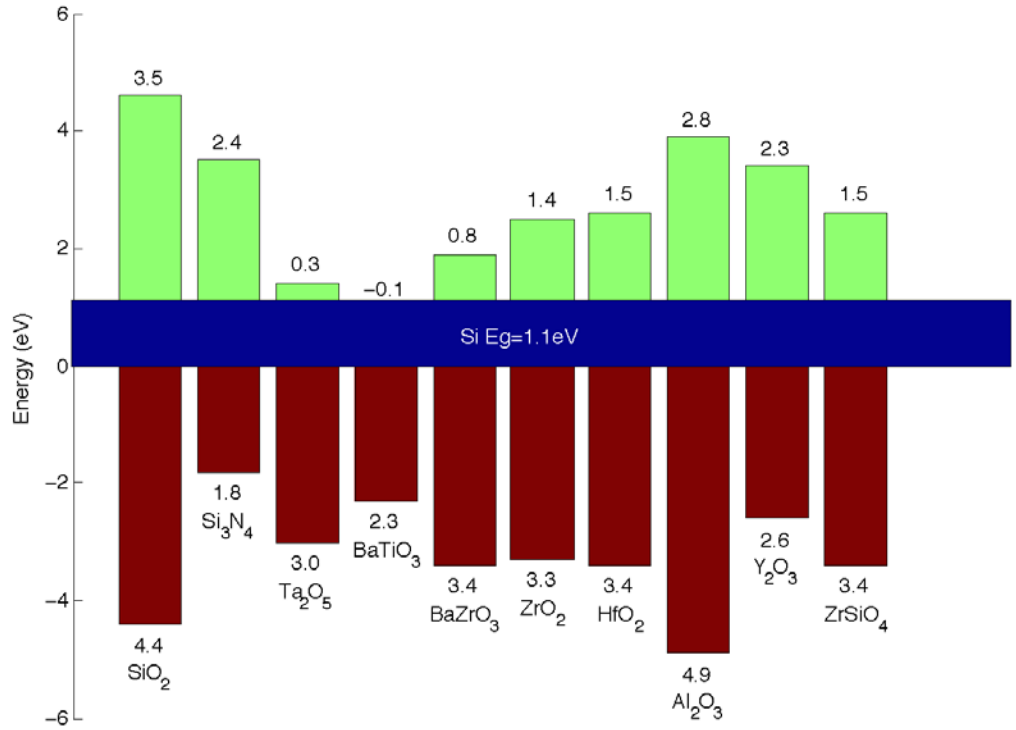


Figure 1.5. Conduction band and valence band offsets of various high-k materials with Si[27].

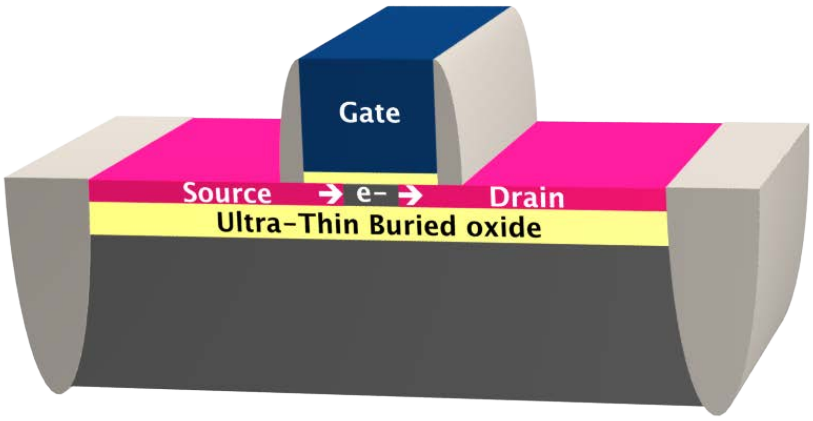
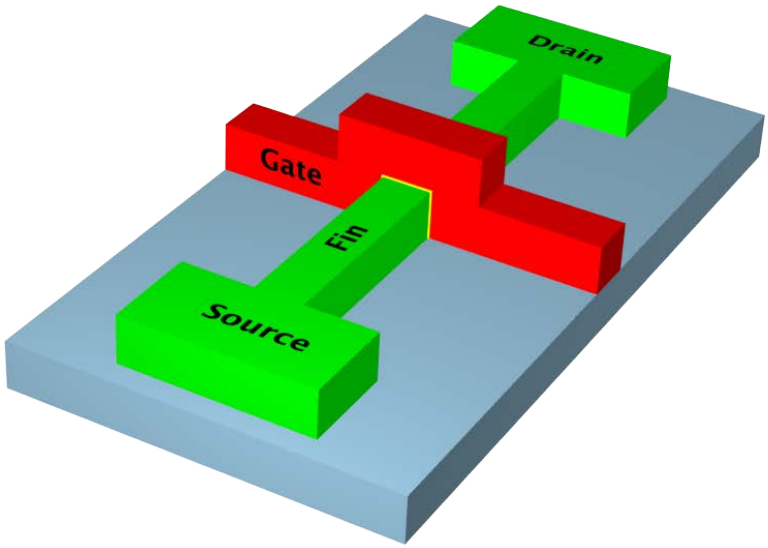
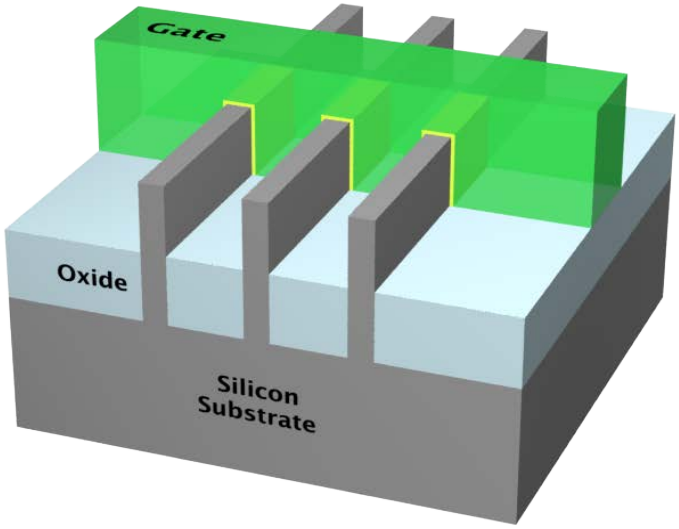


Figure 1.6. The cross sectional view of the fully depleted (FD) silicon-on-insulator (SOI) MOSFETs.

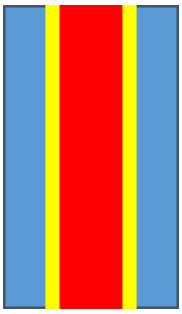


(a)

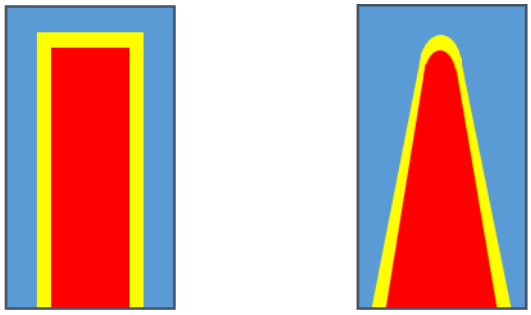


(b)

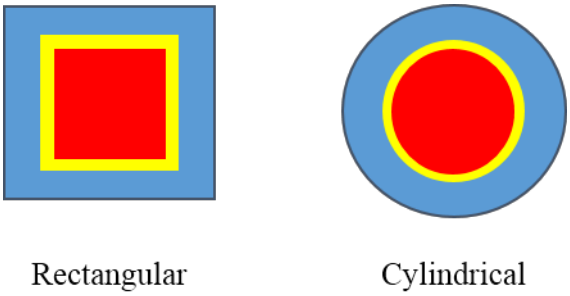
Figure 1.7. (a) The structure of FinFETs. (b) Tri-gate technology by Intel where multiple fins are connected together.



(a)



(b)



(c)

Figure 1.8. Cross sectional views of the conductive channels of (a) double-gate FinFETs (b) Tri-gate transistors (c) gate-all-around transistors

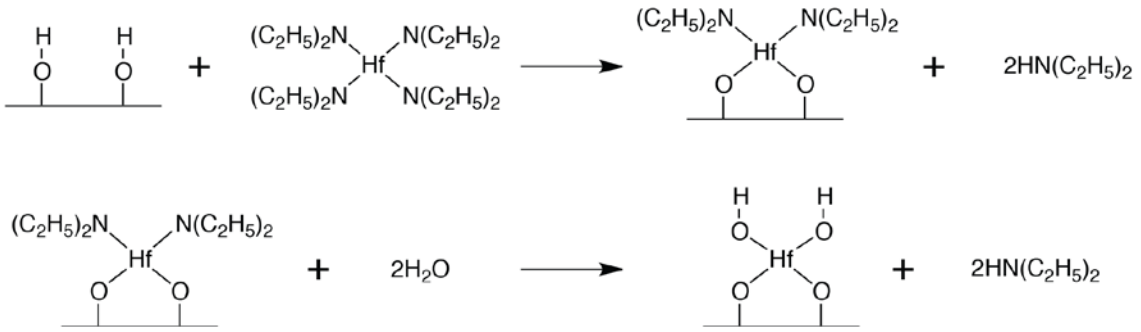


Figure 1.9. Atomic layer deposition of HfO_2 using tetrakis(diethylamino)hafnium (TDMAH) as the precursor and H_2O as the oxidant.

Chapter 2 Fabrication of MOS Capacitors and Improvements

2.1 Introduction

The work in this dissertation focuses on innovations of gate dielectric and dielectric/Si interface in the Metal-Oxide-Semiconductor (MOS) system, and MOS capacitors were fabricated and tested to evaluate the innovations.

MOS devices are the component basis for modern integrated circuit technology. The improvement of performance and stability of the MOS devices enable the tremendous development of integrated circuits and microprocessors. The actual MOS devices in integrated circuits include Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), Complementary MOS devices (CMOS), etc. The MOS capacitor is extensively used in the research of the MOS system because any improvement on the electrical properties of the MOS capacitor makes the same improvement on the actual MOS transistors in the integrated circuits[1]. By measuring the MOS capacitor, we can measure the properties of the gate dielectric, the dielectric/semiconductor interface, the semiconductor substrate, and the metal gate. In a word, nearly all the electrical properties of a MOS system could be measured by measuring the MOS capacitor. The electrical analysis of the MOS capacitor is also simple because thermal equilibrium and one-dimensional treatment apply in this situation[1].

In this Chapter, fabrication of the MOS capacitor is illustrated in details. In addition, a wet etching process for patterning of the metal gate for the MOS capacitor is developed and evaluated; this process is easy to operate, and the contact between the metal and the gate

dielectric is improved comparing to that of the previously established lift-off process. The Si wafers used in our experiments are 2-inch n- and p-type (1 0 0) wafers.

2.2 RCA cleaning

RCA cleaning is a standard set of silicon wafer cleaning steps used in semiconductor manufacturing which needs to be performed before any crucial steps, especially high temperature processing steps, such as rapid thermal process (RTP), dopant activation, etc.

RCA cleaning was firstly developed by Werner Kern in 1965, while he was working for the Radio Corporation of America (RCA)[2]. The purposes of the RCA cleaning, listed following the sequence of the cleaning steps, are to remove organic contaminants (such as dust particles, grease or silica gel) on the wafer surface; then remove silicon oxide that may have built up during the prior steps; finally remove any ionic or heavy metal contaminants[3]

The RCA cleaning procedures of Si wafers are listed as follow:

Step 1: Removal of grease and other organic contaminants.

(1) Acetone cleaning of Si wafers using ultrasonic machine, 3 minutes.

(2) Isopropyl alcohol (IPA) cleaning of Si wafers using ultrasonic machine, 3 minutes

(3) Thoroughly rinse with deionized water (DI H_2O).

Step 2: Removal of native oxide.

(1) Etching Si wafers in a diluted hydrofluoric acid (HF, 49 wt %) solution (DI H_2O: HF=20:1) for 30 seconds.

Check if the surface of the Si wafer is hydrophobic. Bare Si surface should be hydrophobic. If the surface is still hydrophilic, there is remaining SiO_2, and the wafer needs to be etched for extended time.

(2) Thoroughly rinse with running DI H_2O for at least 30 seconds.

Step 3: Removal of organic contaminants (dust particles, grease or silica gel) and metal ionic contaminants (Cu, Ag, etc.) using RCA 1 solution (or SC 1 solution).

(1) Cleaning of Si wafers in RCA 1 solution at 75-80°C for 10 minutes.

The composition of RCA 1 solution is: DI H_2O: NH_4OH (NH_3; 29 wt%.) : H_2O_2 (30 wt%)=5:1:1

(2) Thoroughly rinse with DI H_2O.

Step 4: Removal of chemical oxide grown during RCA 1 cleaning.

(1) Etching in diluted HF solution (DI H_2O: HF=20:1) for 30 seconds. This time is enough to remove chemical oxide grown during RCA 1 cleaning.

(2) Thoroughly rinse with running DI H_2O for at least 30 seconds.

Step 5: Removal of heavy metal contaminants and alkali ions using RCA 2 solution (or SC 2 solution).

(1) Cleaning of Si wafers in RCA 2 solution at 75-80°C for 10 minutes.

The composition of RCA 1 solution is: DI H_2O: HCl (37.9 wt%) : H_2O_2 (30 wt%)=5:1:1

(2) Thoroughly rinse with DI H_2O.

2.3 Growth of gate dielectric

Before the growth of gate dielectric, any silicon oxide built up during the final step of RCA cleaning needs to be removed. Diluted buffered oxide etchant (BOE, 6:1 with surfactant) solution (DI H_2O: BOE=80ml: 20ml) was used, and 1 minute etching time is enough to remove the silicon oxide built up during the RCA 2 cleaning. In this step, BOE solution is preferred to HF solution because Si surface etched by BOE is smoother.

2.3.1 Thermal growth of SiO_2

Various techniques can directly grow or deposit SiO_2 films, such as dry thermal oxidation, wet thermal oxidation, electrochemical anodization, plasma-enhanced chemical vapor deposition (PECVD) and sputtering. Among all the techniques, dry thermal oxidation provides SiO_2 with the best quality and the lowest interface trap densities. Dry thermal oxidation is executed in an elevated temperature and an atmosphere containing dry oxygen (O_2) gas.

For single-crystal Si wafers, the Deal-Grove model is widely accepted to predict the growth of SiO_2 during dry thermal oxidation[4]. However, thin oxides (less than 25 nm) grow much faster than the model predicts.

Growth of ultrathin SiO_2 film (around 20 Å) with good quality could be precisely controlled by dry thermal oxidation using diluted O_2. The oxidation furnace with 3-inch quartz tube is provided by *Lindberg Furnace*. At 900°C, Si wafer was loaded into the

middle position of the quartz tube in nitrogen (N_2) atmosphere. Then N_2 flow rate was set to 1 liter/minute (L/m), and O_2 flow rate was set to 0.2 L/m. O_2 was supplied for 20 seconds. After shutting off the O_2 valve, the temperature of the furnace was maintained at 900°C for another 20 minutes with N_2 keep flowing, in order to anneal the just-oxidized SiO_2 film. Then the furnace was naturally cooled-down. The quartz tube was not opened until the temperature became <400°C, in order to avoid the re-oxidation by the O_2 in the air. The thickness and optical constants (n-refractive index, and k-extinction coefficient) of the SiO_2 film was measured using multi-angle spectroscopic ellipsometer (*J. A. Woollam Co.*, M-2000V model). The setup of spectroscopic ellipsometry is described in *Section 2.8.1*. By following the procedure described above, ~22 Å of SiO_2 could be grown.

2.3.2 Atomic layer deposition of SiO_2 and HfO_2

Atomic layer deposition (ALD) was used to deposit SiO_2 and HfO_2 as gate dielectrics. The details of ALD of SiO_2 and HfO_2 are described in Chapter 4 and Chapter 5.

2.4 Metallization

In the early work of Dr. Chen's group [5-8], Al was deposited by thermal evaporation through a shadow mask to make the MOS capacitor metal gate. Post-metallization anneal (PMA) was needed to decrease interface trap density and make Ohmic contact between Si and Al. Plus, without PMA, an air gap exists between the Al gate and the SiO_2 film, which decreases the accumulation region capacitance value of the MOS capacitor. However, Al is known to diffuse through ultrathin oxides (<30Å) at PMA temperatures (~450°C), causing short-circuit of the MOS capacitor.

Ni has excellent thermal stability (low/negligible diffusion through oxides at PMA temperature). The melting temperature of Ni is high (1455°C), so it can only be deposited by either e-beam evaporation or sputtering. A reliable thickness of metal gate is ~1000Å.

In the MOS capacitors using SiO_2 as the gate dielectric, Ni was used as the gate metal, and the thickness of Ni was 1100Å. Ni contacts tightly with SiO_2, but not with HfO_2. In the MOS capacitors using HfO_2 as the gate dielectric, a thin layer of Ti (100Å) was added between Ni and HfO_2, in order to promote the metal/dielectric adhesion.

2.4.1 Electron-beam evaporation

Electron-beam evaporation was used to deposit metal for the gate of the MOS capacitor, especially gate with multi-layer of metals, because six kind of metal sources can be installed in our electron-beam evaporation system simultaneously. The tooling factor of our electron-beam evaporation system was previously characterized. During deposition, the pressure inside the chamber should be maintained $<10^{-5}$ torr. The deposition rate must be controlled in order to grow metal film with good quality as well as prevent overheating of the substrate.

The desired deposition rates of commonly used metals are listed as follow:

Ni: 0.7~1Å/second

Ti: 0.5Å/second

Al: 1~1.5 Å/second

2.4.2 Sputtering

Sputtering was used to deposit metal and metal nitride. We needed to calculate the tooling factor of each kind of material first: a clean Si wafer was loaded into the sputtering chamber, and half of it was covered by a slice of glass. After deposition, a "step" structure would be formed. Profilometer (*Digital Instruments Veeco Metrology Group,* Dektak 6m model) was used to measure the physical thickness of the "step". The tooling factor of this material should be calculated as:

Tooling factor = profilometer measured thickness / quartz crystal sensor measured thickness.

During the sputtering process, the pressure inside the chamber should be controlled to < 5 mtorr, in order to get thin films with good quality. This consequently puts a limitation on the deposition rate. The desired deposition rates and the corresponding sputtering parameters of commonly used materials are listed in table 2.1.

2.5 Patterning of metal gate

The pattern of the metal gate is circle and the diameter is 100 μm. Our group reported the fabrication of the metal gate using bi-layer-photoresist lithography and lift-off process[9, 10]. However, organic contamination exists between the metal gate and the dielectric. A wet etching process was developed, which is easy to operate, and provides reliable contact between the metal gate and the dielectric.

2.5.1 Previously established lift-off process

The bi-layer-photoresist lithography and lift-off process is shown in figure 2.1, and it is also described as follow:

Step 1: Spin coating of positive photoresist (*Shipley* 1813, *Microchem*) and negative photoresist (SU-8 2001, *Microchem*). The spin speed of S1813 is 2000 rpm, the resulting thickness is ~1.5 μm. The spin speed of SU-8 is 3000 rpm, the resulting thickness is ~1.2 μm. Pre-bake is needed for both of the photoresists.

Step 2: Exposure of the bi-layer photoresists using a contact mask aligner (*Karl Sus*s MJB 3). Exposed photoresists are developed by SU-8 developer (*Microchem*). The SU-8 developer contains 98% 1-Methoxy-2-propyl acetate ($C_6H_{12}O_3$), which is also a solvent for both exposed and non-exposed S1813. When the developer contacts with S1813, it starts to dissolve S1813 both laterally and vertically. Thus, an undercut structure would be formed after the development. A SEM (scanning electron microscope) image of the undercut structure is shown in figure 2.2.

Step 3: Gate metal is deposited using electron-beam evaporation or sputtering.

Step 4: Lift-off of the un-wanted metal using Remover PG (*Microchem*) at 100°C, forming the desired metal gate. The undercut structure of the photoresists makes the lift-off easy to happen, and it also enables sharp metal edge. Increasing the temperature would accelerate the removal of the photoresists. Ultrasonic cleaner could be used to help remove the photoresists and the un-wanted metal if it is needed.

The bi-layer photoresist and lift-off process is easy to operate. Only organic solutions are used in the process, which does not harm the ultrathin dielectric layer at all. However, organic contamination from the photoresist always exists. In the SEM image shown in figure 2.2, organic contamination is left on the Si substrate after development. The contamination frequently causes peeling-off of the metal gate. Even in the samples which did not show peeling-off, the electrical properties of the MOS capacitors would be harmed.

2.5.2 Wet etching process

Efforts have been devoted to develop a metallization first-etching process to make the gate pattern, in order to avoid the organic contamination between the metal gate and the dielectric. After the growth of oxide, Ni was deposited using electron-beam evaporation or sputtering, following by photolithography to make the gate pattern. Then the metal uncovered by the photoresist is going to be etched away in certain solution. Several solutions have been reported as etchants for Ni, such as a mixture of HCl and HNO_3, or a mixture of HF and HNO_3[11]. However, these solutions are acidic and would damage the oxide layer. Iron chloride ($FeCl_3$) solution is an appealing candidate for the etching process, because it etches Ni, meanwhile does not attack oxide[12, 13].

The wet etching process is shown in figure 2.3, and it is also described as follow:

Step 1: Spin coating of positive photoresist (*Shipley* 1813, *Microchem*). The spin speed is 2000 rpm.

Step 2: Exposure of photoresist using a contact mask aligner. Exposed photoresist is developed by MF-319 developer (*Microchem*). The photoresist is going to act as an etching mask.

Step 3: Removal of the native nickel oxide (Ni_xO_y) which is formed by O_2 in the air. The etchant is diluted HCl solution (DI H_2O: HCl=100ml: 50ml), the etching time is 1 minute. In this step, no phenomenon is observable.

Step 4: Removal of Ni using $FeCl_3$ solution. The concentration of the solution is: 150ml DI H_2O: 1g $FeCl_3$. The etching time is 2-3 minutes. In this step, we can easily observe the dissolution of Ni.

Step 5: Removal of the photoresist using Remover PG at 100°C for 10 minutes.

Test has been done to prove the $FeCl_3$ solution does not change the ultrathin SiO_2 dielectric. Thermal SiO_2 was grown on 2 pieces of Si wafers, and the thicknesses of the SiO_2 thin films were measured using multi-angle spectroscopy ellipsometry (SE). On each Si wafer, 2 measuring points were chosen. Then the 2 wafers were etched in the $FeCl_3$ solution for 6 minutes. The thicknesses of the SiO_2 thin films after etching were also measured by SE. All the SE results are listed in table 2.2. There is no obvious increase or decrease of the SiO_2 thickness after etching. The etching time in the test (6 minutes) is longer than the etching time in the actual process (2-3 minutes), so we believe the etching process does not bring any harm to the SiO_2 dielectric in the actual MOS devices.

Native nickel oxide exists on the surface of Ni, and it must be removed before etching Ni. If not, the Ni_xO_y will block the Ni from the $FeCl_3$ solution, and cause failure of forming the metal gate pattern. In figure 2.4 (a), the Ni_xO_y is not removed. The metal gate area is covered by photoresist, and the un-covered Ni area could not be removed by $FeCl_3$ solution. Using ultrasonic cleaner does not promote the etching of Ni, but only causes the peeling-off of the Ni sheet. In figure 2.4 (b), the concentration of the $FeCl_3$ solution is increased. The solution can penetrate through the Ni_xO_y layer and etch Ni, but serious undercut of the Ni gate happens even when there is still Ni residual in the un-covered area. Figure 2.5 is the image of the Ni gate pattern, in which Ni_xO_y was removed first. The shape of the Ni gate is perfect, and the edge is sharp.

MOS capacitors using thermal SiO_2 grown at 900°C as the gate dielectric were fabricated, in order to compare the effects of the gate patterning methods on the electrical properties

of devices. High frequency (100 KHz) Capacitance Density-Voltage (C-V) and Current Density-Voltage (J-V) curves of the MOS capacitors fabricated using both lift-off and wet etching processes were measured, and the results are shown in figure 2.6 and 2.7. The electrical characterization will be discussed in details in Section 2.8.2. The equivalent oxide thicknesses (EOTs) and flatband voltages (V_{FB}) of the MOS capacitors were extracted from the C-V curves by using UC Berkeley's quantum-mechanical C-V simulator. The MOS capacitor characterized in figure 2.6 was fabricated using the lift-off process, the physical thickness of the thermal SiO_2 measured by SE is 2.23nm, and the EOT is 2.24nm. The MOS capacitor characterized in figure 2.7 was fabricated using the wet etching process. The physical thickness of the thermal SiO_2 is 2.22nm, which is comparable to the one in figure 2.6, but the EOT is 1.97nm, which is 0.27nm thinner than the one in figure 2.6. The gate leakage current densities of the MOS capacitors at $V_g=V_{FB}+1V$ are in the same order of magnitude (0.65 A/cm^2 and 0.48 A/cm^2). The shrink of the EOT is attributed to the improved contact between the Ni gate and the SiO_2 dielectric. It also implies the organic contamination between the Ni gate and the SiO_2 introduced by the lift-off process would harm the electrical properties of the device.

In the MOS capacitors using HfO_2 as the gate dielectric, a thin layer (100Å) of Ti was added. The etchant for Ti is diluted HF solution (HF: DI H_2O=5ml: 100ml), and the etching time is 30-45 seconds.

2.6 Back-side contact

Al (1000Å) is deposited onto the back-side of the sample to make the metal contact. Before the deposition, the front-side of the sample is protected by hard baked S1813 (baked at 140°C for 3 minutes), and the sample is etched in pure BOE solution to remove the native silicon oxide on the back-side.

2.7 Annealing

The purpose of annealing is to create an Ohmic contact between Al and the bulk Si, and also passivate the defects in the dielectric layer. Annealing is executed in the annealing furnace with a 3-inch quartz tube (*Lindberg Furnace*) at 450°C in forming gas at the pressure of 1 atmosphere. The flow rate of N_2 is 2 L/min, and the flow rate of H_2 is 0.2 L/min

2.8 Characterization

2.8.1 Multi-angle spectroscopic Ellipsometry

The thickness and optical constants (n-refractive index, and k-extinction coefficient) of the dielectric films could be measured using a multi-angle spectroscopic ellipsometer (*J. A. Woollam Co.*, M-2000V model). The measuring angle range was 45°C to 75°C, and the measuring step was 5°C. The Revs/meas was set to 50, which means 50 times of measurement were taken at each measuring angle, and the average was accepted as the measurement result. The mean squared errors (MSEs) of the measurements in this

dissertation are around 5 or less, indicating good fittings between the experimental data and the models.

2.8.2 Electrical characterization

The Capacitance Density-Voltage (C-V) curve of the MOS capacitor is measured using a HP 4284A precision LCR meter. The equipment is able to measure the C-V curve at frequencies from 1 K to 1 MHz. The Current Density-Voltage (J-V) curve of the MOS capacitor is measured using an Agilent 4155B semiconductor parameter analyzer.

The EOT and the flatband voltage of the MOS capacitor are extracted from the C-V curve using the UC Berkeley Quantum-Mechanical Simulator (taking quantum correction into consideration). The ideal C-V curve is simulated and used to fit the experimental C-V curve. The gate current density of the MOS capacitor is evaluated at the gate voltage $V_G=V_{FB}+1V$.

2.9 Summary

MOS capacitors were fabricated and tested to evaluate the quality of the gate dielectric and the dielectric/Si interface. The details of the fabrication has been elucidated. A wet etching process was developed to make the metal gate. Comparing to the lift-off process, this newly developed wet etching process is easier to operate. Simultaneously, no organic contamination exists between the metal gate and the dielectric, resulting a reliable physical contact and reduced EOT of the device.

Table 2.1. The desired deposition rates and the corresponding sputtering parameters of commonly used materials.

Material	**Power**	**Gas**	**Flow rate**	**Deposition rate**
Ni	100 W	Ar	15 sccm	1-2 Å/sec
Hf	60 W	Ar	15 sccm	0.7-1.6 Å/sec
Au	30 W	Ar	15 sccm	~1.0 Å/sec
Ti	150 W	Ar	15 sccm	1-1.8 Å/sec
TiN	200 W	N_2	15 sccm	~0.5 Å/sec

Table 2.2. Silicon oxide thickness before and after etching in FeCl3 solution for 6 minutes etching. The Mean Squared Error (MSE) of the spectroscopic ellipsometry measurement is <5.

	Thickness before etching	Thickness after etching
Wafer 1 point 1	27.55 Å	26.56 Å
Wafer 1 point 2	27.81 Å	27.07 Å
Wafer 2 point 1	102.18 Å	101.26 Å
Wafer 2 point 2	103.59 Å	103.11 Å

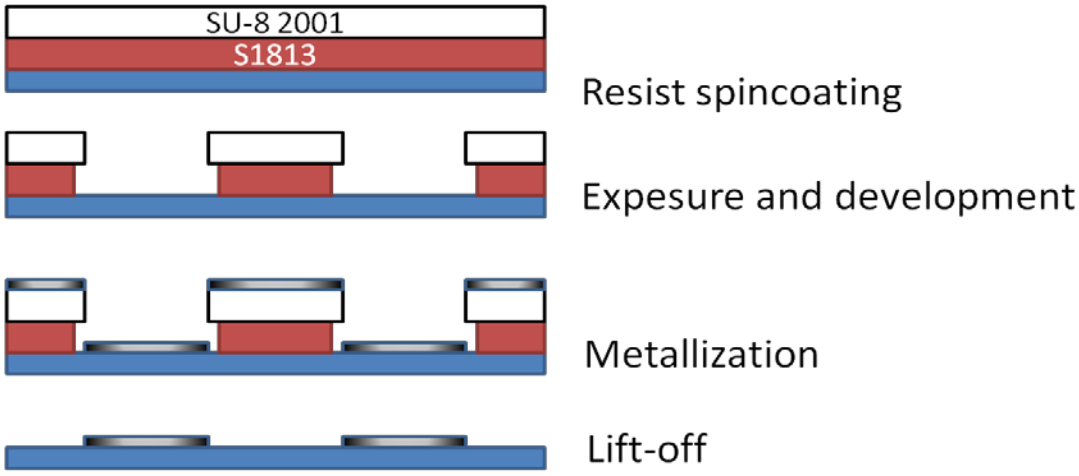


Figure 2.1. The bi-layer-photoresist lithography and lift-off process for making metal gate.

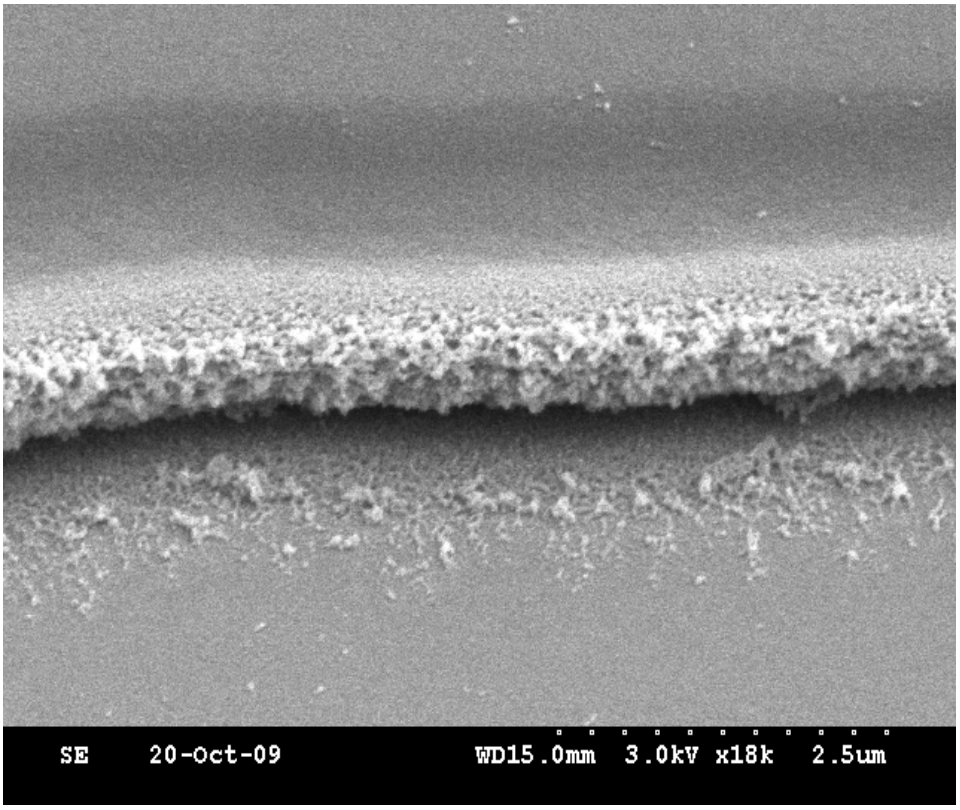


Figure 2.2. The SEM image of the undercut structure.

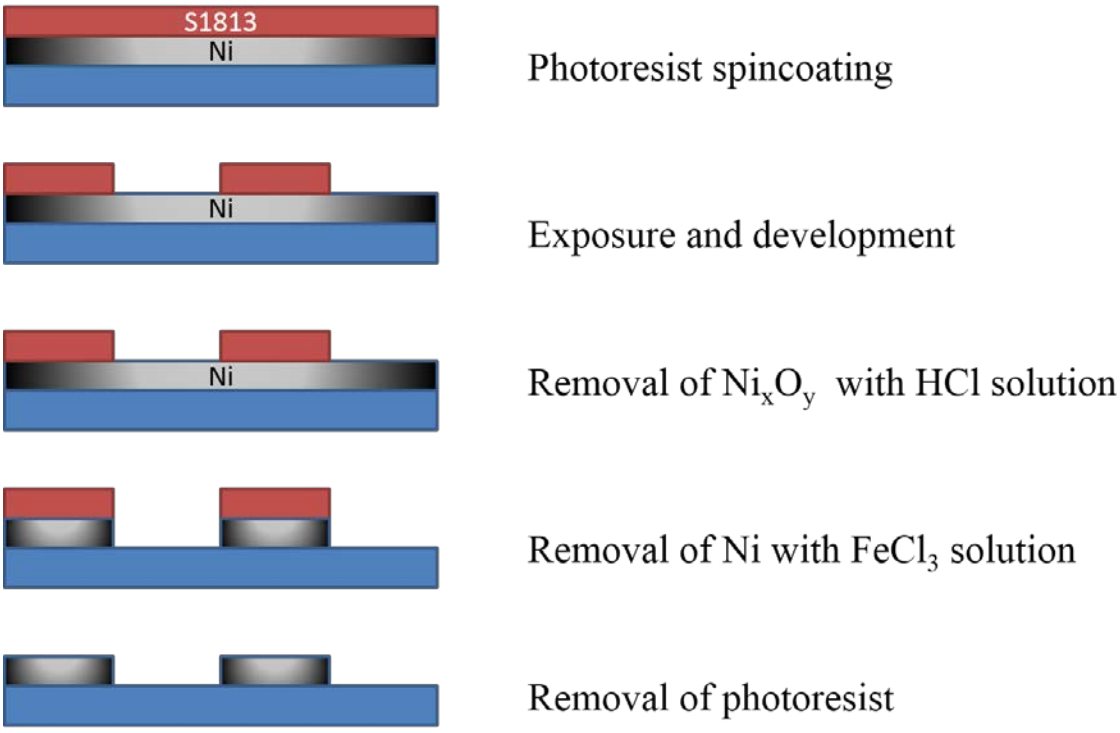


Figure 2.3. The wet etching process for making gate of MOS capacitors using Ni.

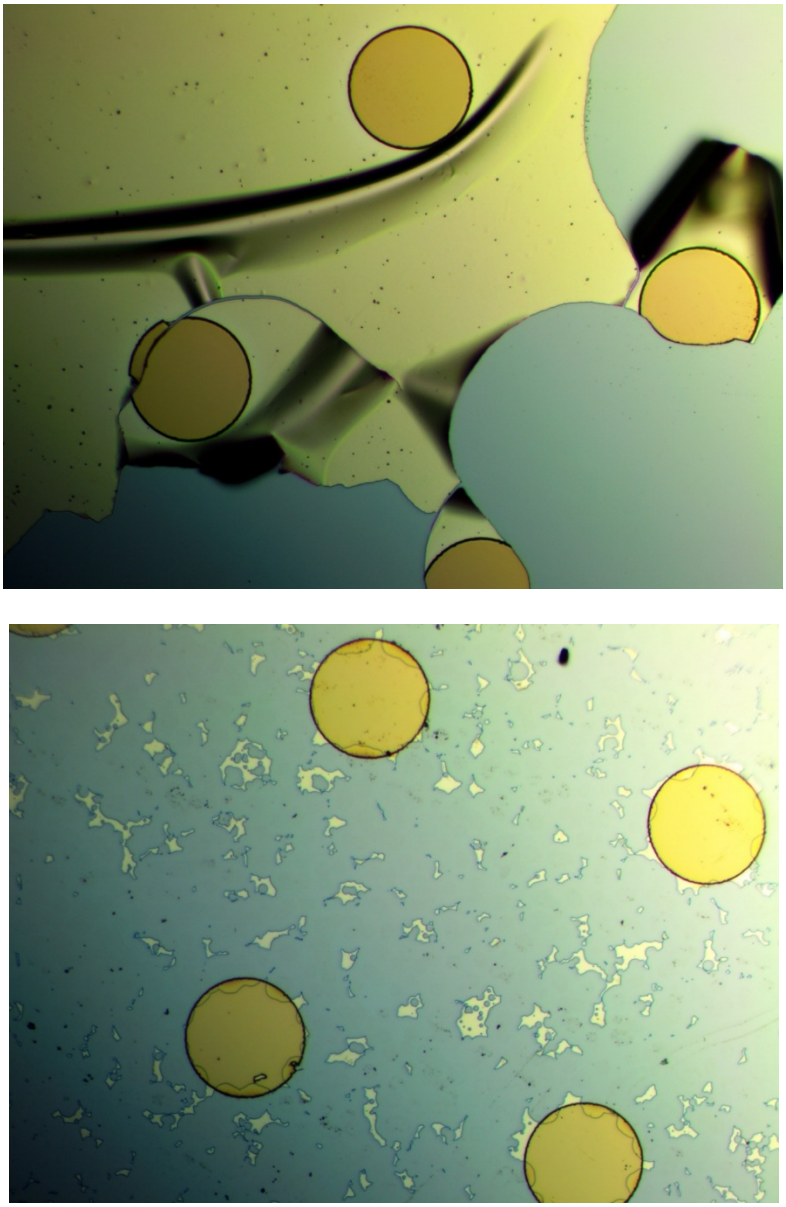


Figure 2.4. (a) Peeling-off of Ni after etching using $FeCl_3$ solution in ultrasonic cleaner. (b) Undercut of Ni gate after etching in $FeCl_3$ solution with higher concentration.

Figure 2.5. Ni gate of MOS capacitors fabricated using wet etching process.

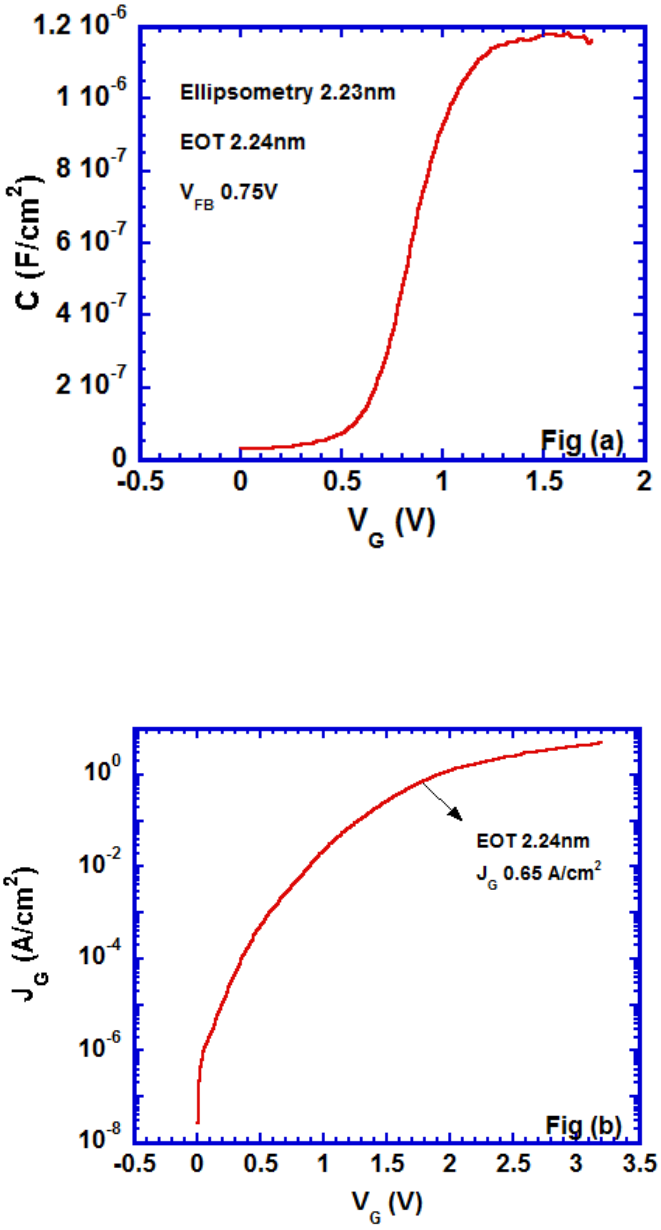


Figure 2.6. (a) High frequency (100 KHz) Capacitance Density-Voltage (C-V) curve and (b) Current Density-Voltage (J-V) curve of a MOS capacitor using thermal SiO2 as the gate dielectric. Lift-off process was used to make Ni gate. The physical thickness of SiO_2 thin film was 2.23nm, and the EOT was 2.24nm.

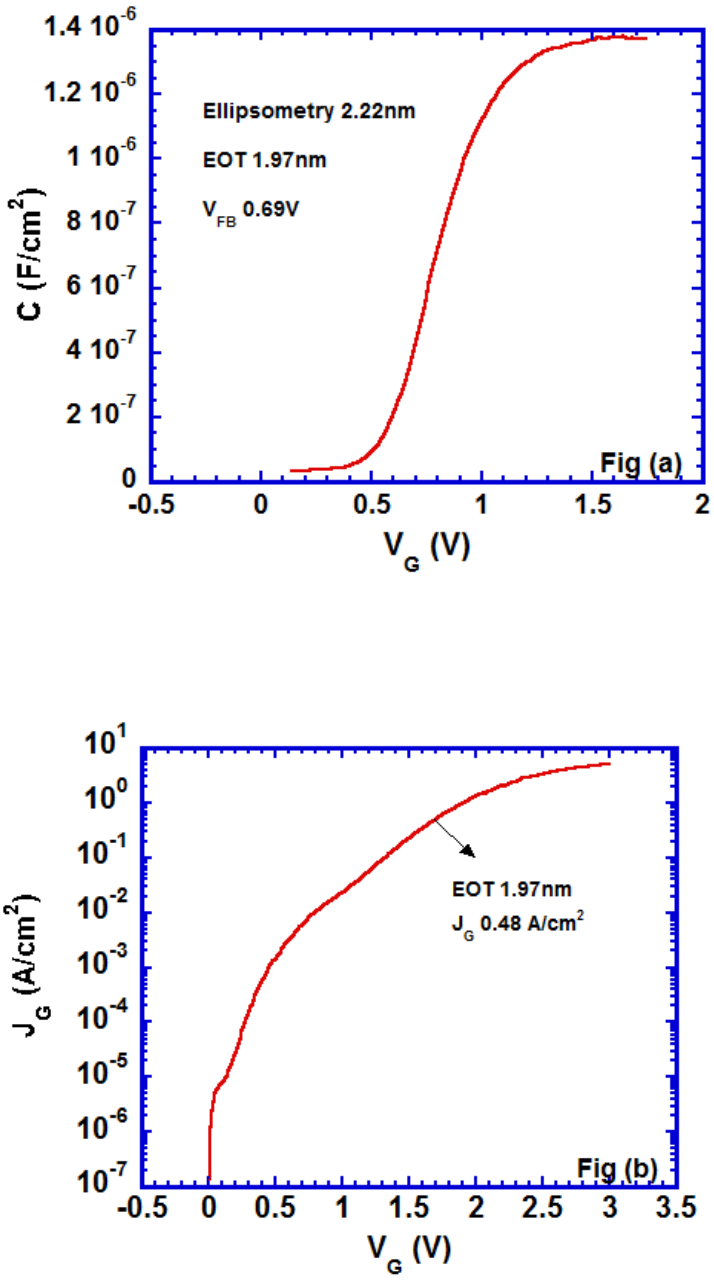


Figure 2.7. (a) High frequency (100 KHz) Capacitance Density-Voltage (C-V) curve and (b) Current Density-Voltage (J-V) curve of a MOS capacitor using thermal SiO2 as the gate dielectric. Wet etching process was used to make Ni gate. The physical thickness of SiO_2 thin film was 2.22nm, and the EOT was 1.97nm.

Chapter 3 Tunneling Current Reduction by Lateral Heating Treatment

3.1 Introduction

Although metal oxides with high dielectric constant (high-k materials) have become the mainstream gate oxide in the complementary-metal-oxide-semiconductor (CMOS) technology, silicon oxide is still unavoidable in MOS devices. Unlike the flawless interface between Si and thermally grown SiO_2, direct deposition of high-k materials on bare Si surface results in high density of interface trap charges and defects, and a SiO_2-based interfacial layer is necessary to improve the interfacial quality. Among various techniques which could be used to deposit high-k materials, atomic layer deposition (ALD) is preferable because of its self-limiting surface reaction. The thickness and the stoichiometry of the high-k dielectric thin films grown by ALD are precisely controlled, and the uniformity of the films is desirable [1-3]. ALD of high-k dielectric materials on bare Si surface without any oxide will be interrupted by nucleation barrier, resulting growth incubation period and additional gate oxide leakage current[4, 5]. A SiO_2-based interfacial layer is necessary for ALD of high-k gate oxide. The essentiality of the interfacial layer in ALD of high-k gate oxide is extensively discussed in Chapter 5. Thus, improvement of the SiO_2 film and the Si/SiO_2 interfacial quality is important.

In this chapter, ultrathin SiO_2 film was thermally grown. Using a lateral heating treatment of the ultrathin SiO_2 film, the gate leakage current of the SiO_2 based MOS capacitors is reduced by 4-5 orders of magnitude, and the underlying mechanism is investigated. In Chapter 7, the SiO_2 film which went through the regular rapid thermal process (RTP) (not

the lateral heating treatment) is controllably etched by diluted hydrofluoric acid (HF) solution, and the etched SiO_2 film is used as an interfacial layer for ALD of HfO_2.

3.2 Setup of the Rapid Thermal Process (RTP) system

The lateral heating treatment was executed in a Rapid Thermal Processing (RTP) system (RTP-600S) from *Modular Process Technology Corp.* RTP is a standard semiconductor manufacturing process, and it is commonly used for semiconductor processing techniques such as rapid thermal oxidation, dopant activation, rapid thermal annealing, etc. In our RTP system, samples are held in a quartz chamber. The energy source is the light radiation from two banks of linear tungsten-halogen lamps. One bank of the lamps is located on top of the quartz chamber, and the other bank is located below the quartz chamber. The temperature is controlled by a close-loop pyrometer controller, and each new control file needs to be calibrated using a high temperature thermocouple (type K). The flow rates of the gases in the chamber are controlled by the built-in mass-flow-controllers (MFC).

The processing gas used in RTP is helium (He) or nitrogen (N_2), which are inactive with Si at elevated temperature. The temperature trails of the RTP using both processing gases were monitored by a thermocouple, and it was found that He cools down the quartz chamber faster than N_2 does. Before the increase of the temperature, the chamber is purged by a large flow of He or N_2 (flow rate = 20 liter/minute), in order to get rid of the air residual. The temperature in the chamber ramps up at a rate of 10°C/second, until it reaches the desired processing temperature (1000°C-1100°C). SiO_2 decomposes at

temperature >1000°C[6], so trace O_2 is needed in the processing gas in order to prevent the decomposition of the ultrathin SiO_2 film. The common concentration range of the trace O_2 is 200-500 parts-per-million (ppm). After a certain period of time (from several seconds to a few minutes), the lamps are shut down, and the chamber starts to cool down. At this step, the large flow of purging gas is turned on again. Compressed air and chilled water flow around the quartz chamber in the whole process, in order to prevent the equipment from being overheated, and to help the chamber to cool down. It takes about 5 minutes for the temperature inside the chamber to decrease from ~1100°C to below 100°C.

The gas route of the RTP system is displayed in figure 3.1. He or N_2 is split into two paths, one is the purging gas, which goes directly into the RTP system, and is controlled by a built-in MFC (not shown in the figure); the other one is the processing gas, and is controlled by the flow meter 1. The flow rate of the flow meter 1 is set to 1.5 L/min. O_2 is controlled by the flow meter 2, and the flow rate of the flow meter 2 is adjustable, in order to get the desired trace O_2 concentration of the mixed gas. The mixed gas flows into the RTP chamber, and is controlled by another built-in MFC (not shown in the figure). Compressed air flows around the quartz chamber to cool down the chamber and the equipment.

The temperature inside the quartz chamber is above 1000°C during the RTP. At this temperature, Si will be easily oxidized by the trace O_2 and trace moisture in the processing gas. Thus, the concentrations of O_2 and moisture in the processing gas must be precisely monitored. The concentration of O_2 is measured using a trace O_2 analyzer (Alpha Omega

Series 3000) with a measurement range of 1-10000 ppm, and the concentration of moisture is measured using a dew point meter (JLC International Shaw Inline Dew Point Meter).

The processing gas could be monitored either at the gas entrance or at the gas exhaust port of the RTP chamber, controlled by valve 1 and valve 2. Valve 1 is an on-off valve, and vale 2 is a 3-way valve. When valve 1 is opened and valve 2 is closed, a bypass of the processing gas flows through the trace O_2 analyzer and the dew point meter. The flow rate of O_2 is adjusted according to the measurement result of the trace O_2 analyzer, until the desired O_2 concentration is achieved. When valve 1 is closed and valve 2 is switched to the trace O_2 analyzer, the exhaust gas flows through the trace O_2 analyzer and the dew point meter before it enters into the atmosphere. Ideally, if the seal of the RTP chamber is perfect, the O_2 and moisture concentrations of the processing gas measured at the gas entrance and at the gas exhaust port of the RTP chamber should be the same. If the quartz chamber has a gas leakage, the O_2 and moisture concentrations measured at the gas exhaust port would be increased. Thus, by monitoring the exhaust gas, we can get an alarm when there is gas leakage in the chamber.

Before running a RTP file, both valve 1 and valve 2 are closed. All processing gas goes into the quartz chamber, in order to form a stable gas ambience.

3.3 Lateral heating treatment

In order to realize the lateral heating treatment of the Si wafer using the RTP system, a "sandwich" structure was designed. The top view and the side view of the structure are shown in figure 3.2. A 4 inch Si wafer is used as the substrate holder. A quarter of a 2 inch Si wafer is used to support the sample, and is named as the Si supporter 1. The Si sample is cut into a rectangle, which is much smaller than the substrate holder. The sample is mounted onto the Si supporter 1, and the location is adjusted so that the edge area of the Si sample is hanged up. The hanging area is a rectangle, the length and width of which are roughly controlled. A piece of long and narrow rectangular Si is mounted onto the middle area of the sample, in order to support the radiation blocker, and is names as the Si supporter 2. The radiation blocker is also a piece of Si with rectangular shape, which is slightly larger than the sample. The radiation blocker is mounted onto the Si supporter 2, and the location is adjusted so that it thoroughly covers the sample.

In this structure, the sample is completely isolated from the light radiation, and heat transfers between the directly contacted Si wafers. The generation of heat is dependent on the area exposed to the light. The exposed area of the substrate holder is much larger than other components in the structure, so most heat is generated in the substrate holder, and the temperature of the substrate holder is the highest. No heat is generated in the sample by the light radiation, and heat flows from the substrate holder through the Si supporter 1 to the sample. The heat flows laterally in the sample from the contact area to the hanging edge area. A part of the heat also flows from the sample through the Si supporter 2 to the radiation blocker. Since the Si supporter 2 is narrow, only a small amount of heat is

transferred to the radiation blocker. Temperatures of several components of the sandwich structure were measured by a high temperature TC, and it was found that when the temperature of the substrate holder is 1090°C, the temperature of the sample is 1050°C, and the temperature of the radiation blocker is 1030°C. The lateral heat flow in the sample is drawn in figure 3.2 (b).

Using the sandwich structure, heat flows laterally from the contact area to the hanging edge area in the Si sample. Material structure changes after the lateral heating treatment, and will be discussed in the section 3.5.

3.4 Experimental

Ultrathin SiO_2 film was thermally grown on a 2 inch Phosphorus doped n type Si (100) wafer with a resistivity of 1-20 Ω cm. The oxidation was executed in diluted O_2 (N_2: O_2=5: 1) at 900°C for 20 seconds, followed by a post-oxidation annealing for 20 minutes. The details of the oxidation process is described in Section 2.3. The physical thickness of the ultrathin SiO_2 film was ~2.3 nm (measured by multi-angle spectroscopic ellipsometry). The wafer was then cut into two parts, one part was cut into a rectangle and was processed using the lateral heating treatment, and the other part was used as the control sample. The processing gas was He with trace O_2. The trace O_2 concentration of the processing gas was 195 ppm, and the dew point was -54.2°C. The temperature of the RTP quartz chamber was increased to 1060°C at a rate of 10°C/second, then held at 1060°C for 10 seconds.

MOS capacitors were fabricated to electrically characterize the Si/SiO_2 material structure change after the lateral heating process. 1000 Å of Nickel (Ni) was deposited as gate metal by electron-beam evaporation. The gate was patterned using photolithography and lift-off. The details of this process were described in Chapter 2. The gate patterns were circles and the diameter was 100μm. Back contact was made by 1000 Å aluminum (Al), which was also deposited by electron-beam evaporation. The sample was annealed at 450^0C in forming gas for 30 minutes, which created an Ohmic contact between Al and the bulk Si, and also passivated the defects in the SiO_2 layer.

The capacitance density-voltage (C-V) curves of the MOS capacitors were measured using an Agilent 4284A LCR meter at 100 KHz, and the current density-voltage (J-V) curves were measured using an Agilent 4155B semiconductor parameter analyzer. Equivalent Oxide Thickness (EOT) and flatband voltage (V_{FB}) were extracted from the C-V curves by UC Berkeley's quantum-mechanical C-V simulator.

3.5 Results and discussion

3.5.1 Gate leakage current reduction after lateral heating treatment

After lateral heating treatment, the thickness of the ultrathin SiO_2 film were measured by multi-angle spectroscopic ellipsometry. The physical thicknesses of the SiO_2 in the hanging edge area and the contact area are 23.86 Å and 23.88 Å (measured by multi-angle spectroscopic ellipsometry, MSE<5). Comparing to the physical thickness of the SiO_2 before lateral heating treatment (~23Å), the regrowth of the SiO_2 is negligible. This is attributed to the low concentrations of trace O_2 and moisture in the processing gas.

High frequency (100 KHz) Capacitance density-Voltage (C-V) curves and Current density-Voltage (J-V) curves of the MOS capacitors are displayed in figure 3.3 (a) and (b). Three capacitors were measured from the control sample (the red curves in the figures), one capacitor was measured from the contact boundary in the lateral heating treatment (LHT) sample (the green curves in the figures), and three capacitors were measured from the hanging edge area in the lateral heating treatment sample (the blue curves in the figures). They are the representatives of 10-20 measured capacitors from each location. The simulated EOTs and V_{FB}s are marked in figure 3.3 (a), and are also listed in table 3.1 to compare. The gate leakage current densities of the capacitors are evaluated at $V_G=V_{FB}+1V$, and are listed in table 3.1.

When the thickness of SiO_2 is < 3 nm, the gate leakage current is mainly direct tunneling current. The direct tunneling current depends exponentially on SiO_2 thickness, every 0.2 nm thickness increase corresponds to 1 order of magnitude tunneling leakage current reduction. The EOTs of the three MOS capacitors from the control sample are 2.34 nm, 2.29 nm and 2.22 nm, the corresponding gate leakage current densities at $V_G=V_{FB}+1V$ are 1.06 A/cm^2, 0.13 A/cm^2 and 0.13 A/cm^2. The gate leakage currents match well with the reported gate leakage current of thermally grown SiO_2 [7-9]. The EOT of the MOS capacitor from the contact boundary in the lateral heating treatment sample is 2.33 nm, which is comparable to the thickest EOT of the control sample (2.34 nm) and ~0.1 nm thicker than the thinnest EOT of the control sample (2.22 nm). The corresponding gate leakage current density is 1×10^{-2} A/cm^2. Even if we take the 0.1 nm thicker EOT into

consideration, the gate leakage current density is still 1 order of magnitude lower than those of the control sample. The EOTs of the MOS capacitors from the hanging edge area in the lateral heating treatment sample are 2.24 nm, 2.32 nm and 2.37 nm, which are comparable to the EOTs of the control sample. The corresponding gate leakage current densities are 3.7×10^{-6} A/cm^2, 1×10^{-6} A/cm^2 and 1.2×10^{-6} A/cm^2, which are 4-5 orders of magnitude lower than those of the control sample. Since the effect of the increased EOT has been excluded, the reduction of the gate leakage current is attributed to the lateral heating treatment.

The most remarkable phenomenon is that, there is a strong correlation between the flatband voltage (V_{FB}) shift and the direct tunneling leakage current reduction. The average V_{FB}s of the MOS capacitors from the control sample, the contact boundary in the lateral heating treatment sample, and the hanging edge area in the lateral heating treatment sample are ~0.7 volts, 0.38 volts and ~0.2 volts. The V_{FB} shifts towards the negative direction after the lateral heating treatment, the largest V_{FB} shift appears in the hanging edge area, and the corresponding leakage current reduction in this area is also the most significant. Effort has been devoted to explore the underlying mechanism of the V_{FB} shift and the corresponding tunneling leakage current reduction.

3.5.2 Analysis of flatband voltage (V_{FB}) shift

The flatband voltage of MOS capacitors is described by the following equation[10]:

$$V_{FB} = \Phi_{MS} - \frac{Q_{it}}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{T_{ox}} \frac{x}{T_{ox}}\rho(x)dx \qquad (3.1)$$

where $q\Phi_{MS} = q\Phi_M - q\Phi_S$ is the work function difference between the gate metal (Ni in our experiments) and the substrate material (Si); Q_{it} is the interface trap charge density; C_{ox} is the gate oxide capacitance density; T_{ox} is the gate oxide physical thickness; and $\rho(x)$ is the gate oxide charge density, which is distributed along the gate oxide thickness. There are five independent variables in this equation which have influence on the V_{FB}: Φ_M, Φ_S, Q_{it}, C_{ox} (or T_{ox}) and $\rho(x)$. They are going to be discussed individually.

The gate metal is deposited after the lateral heating treatment, so the metal work function ($q\Phi_M$) of the lateral heating treatment sample should be the same with that of the control sample. The V_{FB} shift is not caused by the change of the $q\Phi_M$.

As discussed above, the physical thicknesses and EOTs of the control sample and the lateral heating treatment sample are comparable, indicating the C_{ox} of both samples are also comparable. The large V_{FB} shift (0.5 V) in the hanging edge area could not be attributed to the change of the C_{ox} (or T_{ox}).

The gate oxide charge density ($\rho(x)$) could be changed by contamination, and the oxygen vacancies repairing by the trace O_2 during the lateral heating treatment. Is it possible that additional contamination was introduced into the sample during the lateral heating process? Referring to table 3.1, the V_{FB} shift is large in the hanging edge area (from 0.7 V to 0.2 V), but is smaller in the contact boundary area (from 0.7 V to 0.38 V). If there is additional contamination during the lateral heating treatment, it should be spread all over the sample

by the high temperature, and the amplitudes of the V_{FB} shifts in different area of the sample should be the same. The non-uniform V_{FB} shift indicates the sample is not contaminated by the lateral heating treatment. Is it possible that the V_{FB} shift is caused by the repair of the oxygen vacancies? The oxygen vacancies are positive charges in SiO_2. When they are repaired, the positive charges in the SiO_2 is reduced, and according to equation 3.1, the V_{FB} should be shifted towards the positive direction. However, this is opposite to the experiment results, where the V_{FB} shifts towards the negative direction. Based on the analysis above, the V_{FB} shift is not caused by the change of the $\rho(x)$.

The common interface trap density N_{it} of the thermal SiO_2-Si interface is ~2×10^{10}/cm^2 [11-13], and the corresponding interface trap charge density $Q_{it}=qN_{it}$ is ~3.2×10^{-9}C/cm^2. The shift of the V_{FB} caused by the change of the Q_{it} is described as

$$\Delta V_{FBit} = -\frac{\Delta Q_{it}}{C_{ox}} \tag{3.2}$$

As displayed in figure 3.3 (a), the average C_{ox} of the MOS capacitors in the hanging edge area is ~1.25×10^{-6} F/cm^2. If the 0.5 V ΔV_{FB} in the hanging edge area is caused by the change of the Q_{it}, the corresponding ΔQ_{it} would be 6.25×10^{-7}C/cm^2, which is more than 2 orders of magnitude higher than the original Q_{it} of the control sample. If this is the actual situation, the C-V curve would be deformed by the large amount of the interface traps. However, the C-V curves in figure 3.3 (a) are in good shape. No apparent difference of C-V curves was observed between the lateral heating treatment sample and the control sample, indicating their comparable interfacial qualities. This result suggests that the change of the Q_{it} is not the reason for the V_{FB} shift.

There is only one possible reason left for the V_{FB} shift, which is the change of the Si work function (Φ_S). The Si structure must have been changed after the lateral heating treatment, and the Si work function have been correspondingly modified. During thermal oxidation, a transition layer of SiO_2 exists at the Si-SiO_2 interface. The large volume expansion of the SiO_2 in the transition layer introduces tensile stress to the Si, and compressive stress to the SiO_2 [14-16]. The Si lattice at the interface is distorted by the tensile stress, and the thickness of the distorted Si layer could be more than 2 nm[17]. In the conventional oxidation using the furnace, most of the stress might be released by the slow heating up and cooling down processes, while in the lateral heating treatment using the RTP, most of the stress might be preserved by the rapid heating up and cooling down processes. The appealing electrical properties of the lateral heating treatment sample indicates that a strained Si layer with tensile stress might be formed at the Si-SiO_2 interface, and the corresponding work function Φ_S is modified.

3.5.3 Underlying mechanism of the gate leakage current reduction

The mechanism of the transportation of electrons across the ultrathin dielectric can be classified into two categories: (1) Fowler-Nordheim (FN) tunneling, in which the electrons tunnel through a triangular potential barrier into the conduction band of the gate oxide; (2) direct tunneling, in which the electrons tunnel through a trapezoidal potential barrier into the metal gate[18-21]. The energy band diagrams of the two tunneling mechanisms are drawn in figure 3.4[22]. For each mechanism, the tunneling probability of an electron is

dependent on the thickness of the oxide and the potential barrier height. For SiO_2 films < 0.3 nm, the electrons tunneling mechanism is mainly the direct tunneling.

It was inferred in Section 3.5.2 that the change of the Si work function (Φ_S) is the reason for the V_{FB} shift. Based on equation 3.1, the V_{FB} shift could be described by

$$\Delta V_{FB} = -\Delta\Phi_S \tag{3.3}$$

The V_{FB} shifts towards the negative direction, so the Φ_S must have been increased. The energy band diagram of the MOS capacitor is displayed in figure 3.5, and the scales of the modified energy band at the Si-SiO_2 interface are marked out in red color. As discussed in Section 3.5.2, only the Si structure near the Si-SiO_2 interface is changed. If the Φ_S at the Si-SiO_2 interface is increased, the conduction band E_c of the Si must have been decreased. In order to investigate the effect of the lateral heating treatment on the valence band E_v of the Si, p-type Si based MOS capacitors were fabricated and studied in our group[23]. No V_{FB} shift was observed in the C-V curves of the p-type Si based MOS capacitors, indicating an unaltered valence band E_v.

Based on the analysis above, the underlying mechanism of the gate leakage current reduction is revealed: after the lateral heating treatment, a strained Si layer with tensile stress is formed at the Si-SiO_2 interface. The conduction band E_c of the strained Si layer is decreased, and the valence band E_v is unaltered. Comparing to the bulk Si, the energy band gap of the strained Si layer is narrower. The potential barrier height between the interfacial Si and the SiO_2 is increased, resulting the direct tunneling current reduction.

3.6 Conclusion

Using a lateral heating treatment of the thermally grown ultrathin SiO_2 film, a thin layer of strained Si is formed at the Si-SiO_2 interface, the potential barrier height between the strained Si and the SiO_2 is increased, and the gate leakage current of the corresponding MOS capacitors is reduced by 4-5 orders of magnitude.

Table 3.1. Comparison of electrical properties of MOS capacitors from the control sample, the contact boundary in the lateral heating treatment sample, and the hanging edge area in the lateral heating treatment sample.

Capacitors location	Capacitors number	EOT (nm)	V_{FB} (V)	$J_G@V_{FB}+1V$ (A/cm^2)
Control sample	1	2.34	0.65	1.06
	2	2.29	0.68	0.13
	3	2.22	0.71	0.13
LHT sample contact boundary	1	2.33	0.38	1×10^{-2}
LHT sample hanging edge area	1	2.24	0.19	3.7×10^{-6}
	2	2.32	0.2	1×10^{-6}
	3	2.37	0.22	1.2×10^{-6}

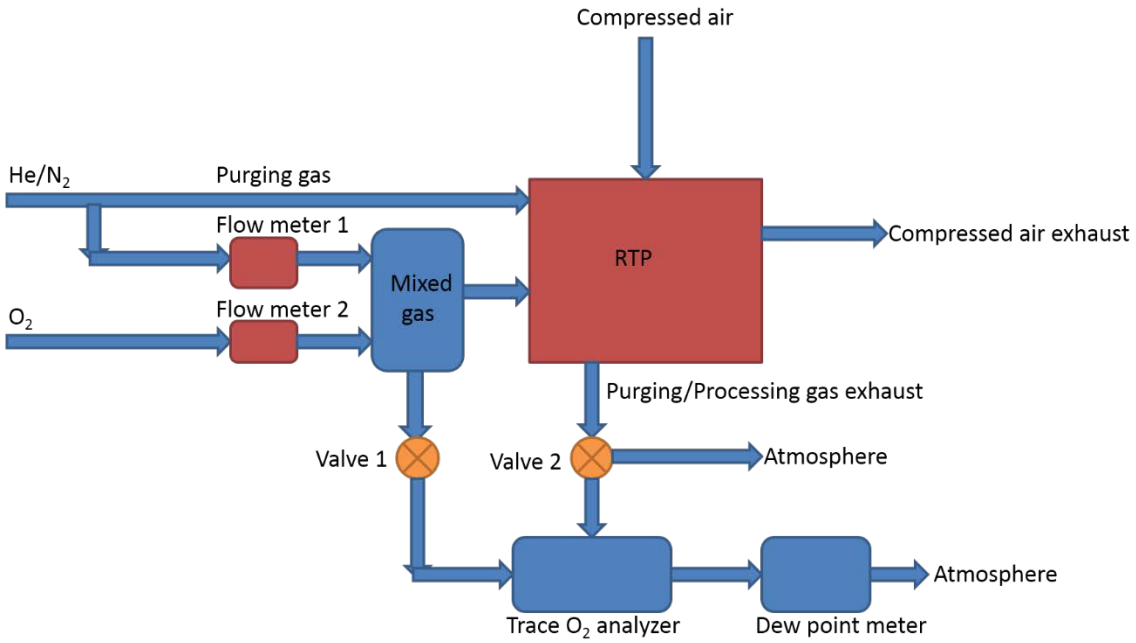


Figure 3.1. Gas route of the RTP system. O_2 analyzer and dew point meter are connected to control the trace O_2 concentration and the humidity in the processing gas.

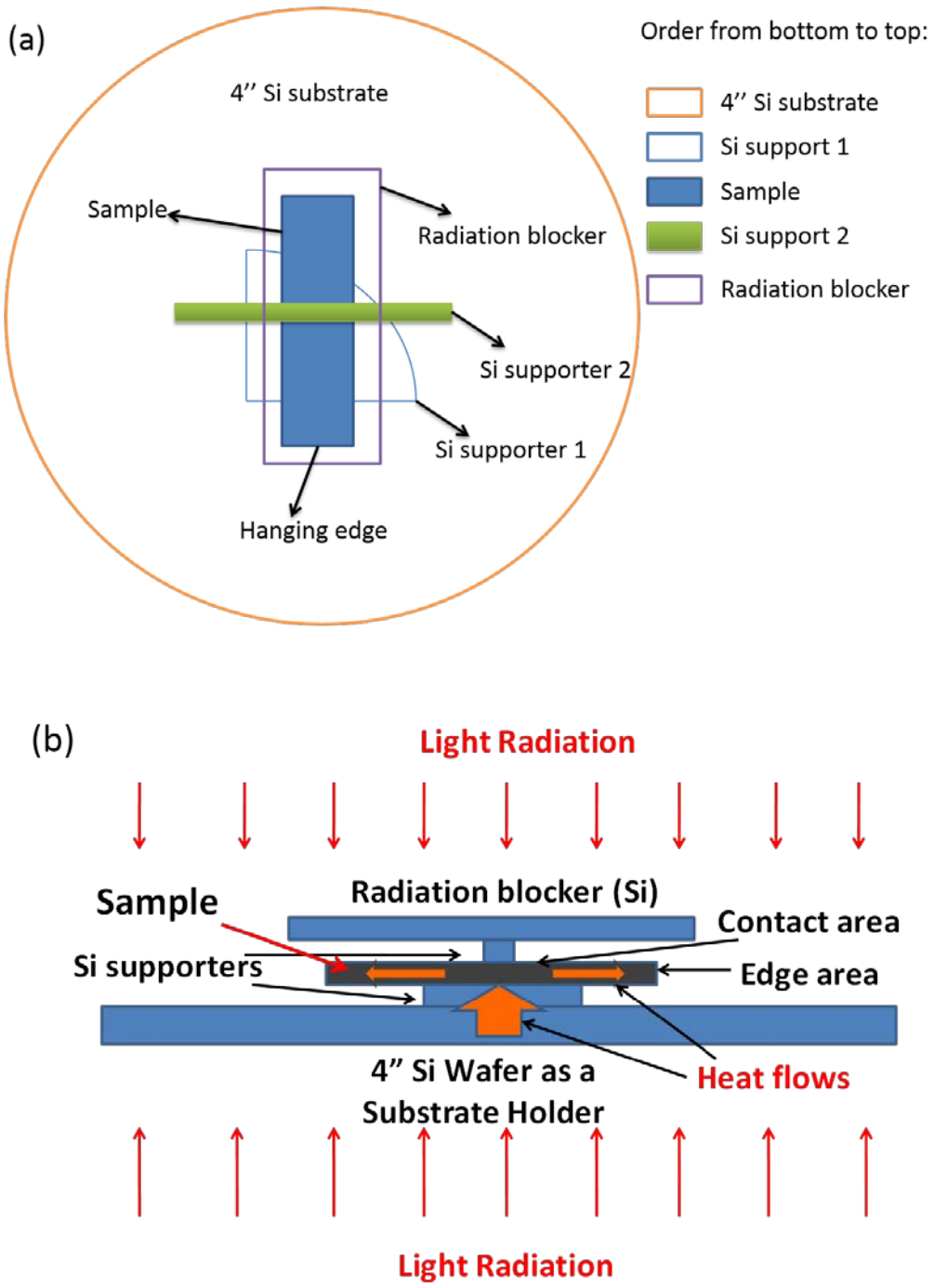


Figure 3.2. (a) The top view and (b) the side view of the sandwich structure for lateral heating treatment.

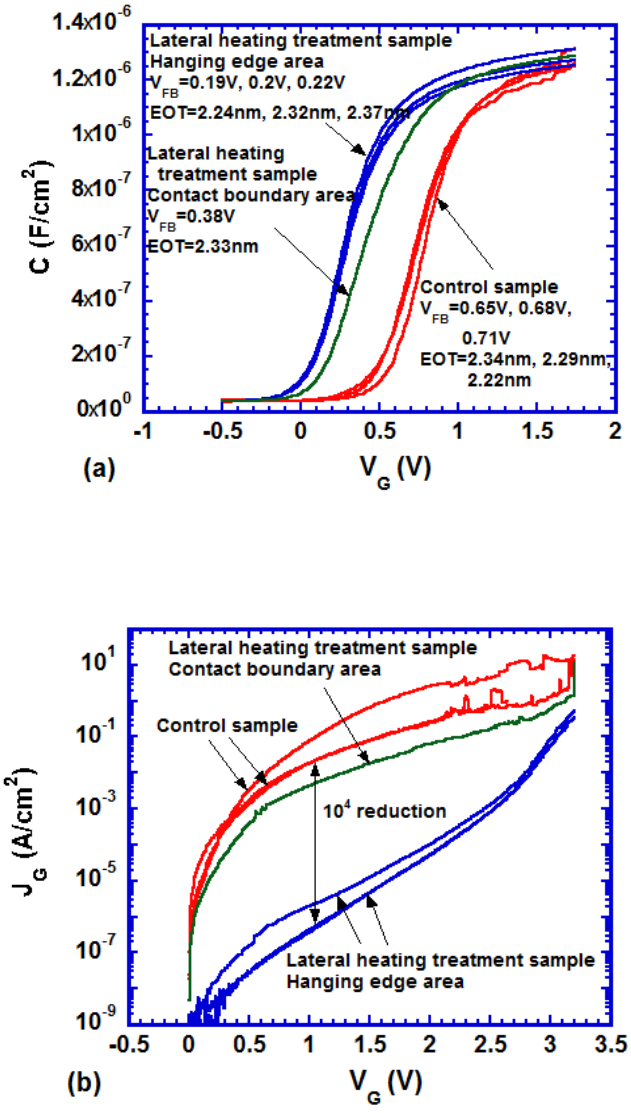


Fig 3.3. (a) High frequency (100 KHz) Capacitance density-Voltage (C-V) curves and (b) Current density-Voltage (J-V) curves of MOS capacitors with and without lateral heating treatment. 3 capacitors were measured from the control sample, 1 capacitors were measured from the lateral heating treatment sample near the contact area, and 3 capacitors were measured from the lateral heating treatment sample hanging edge area. They are the representatives of 10-20 measured capacitors from each location.

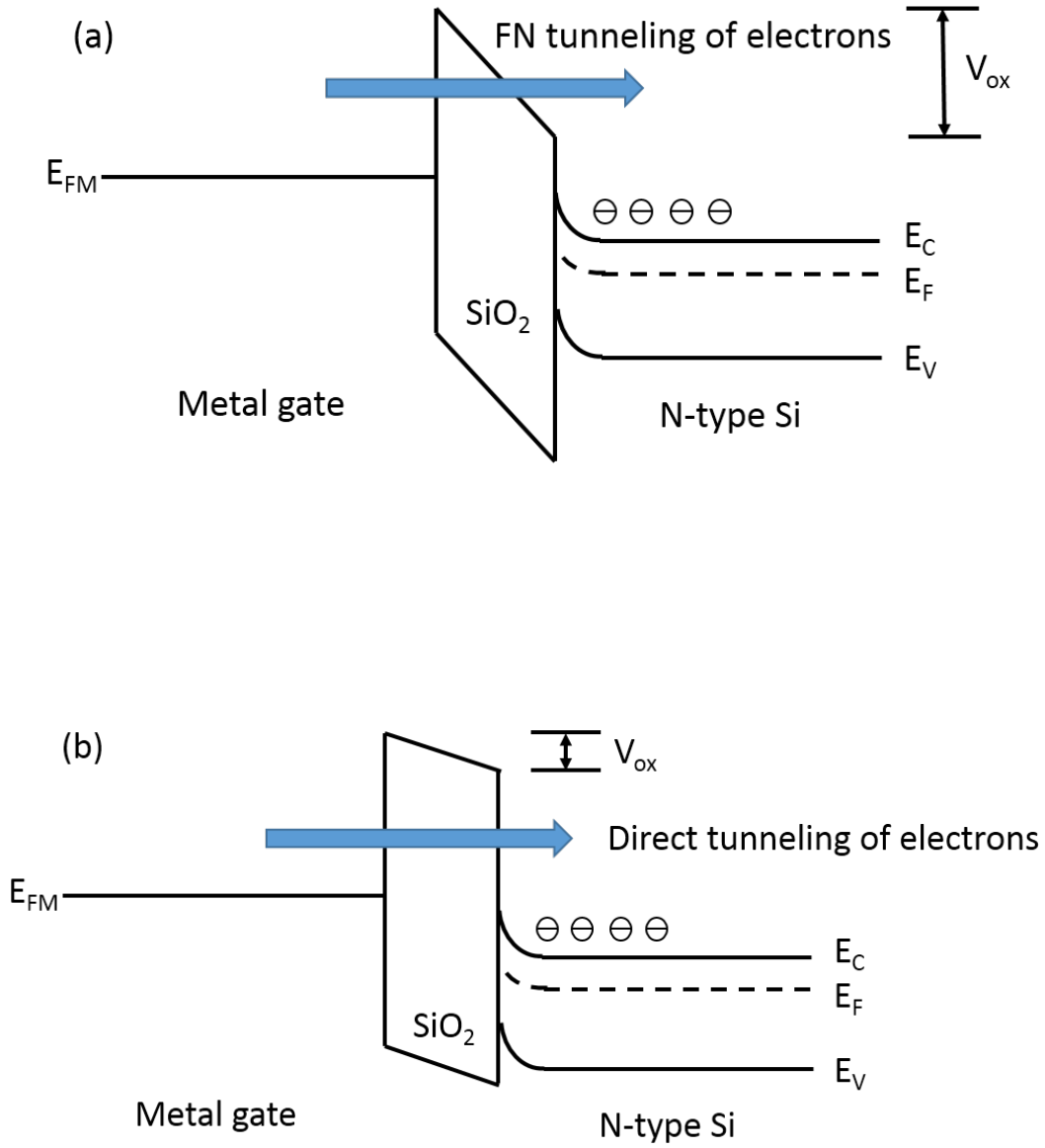


Figure 3.4. Tunneling mechanisms of electrons across the ultrathin SiO_2 film on an n-type Si substrate. (a) Fowler-Nordheim (FN) tunneling. (b) Direct tunneling.

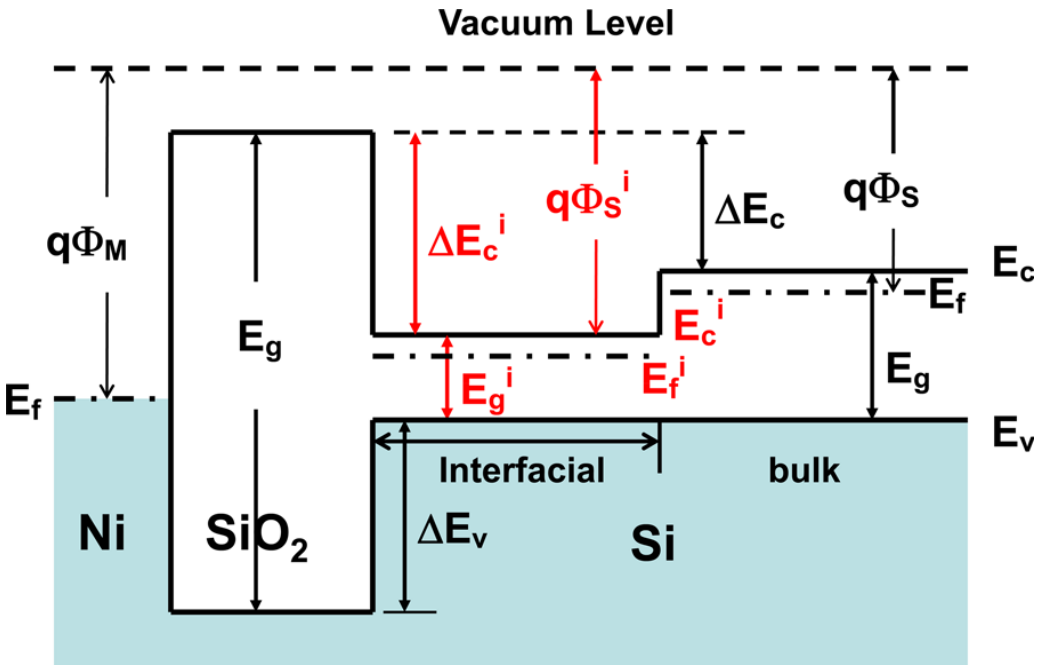


Figure 3.5. The energy band diagram of an N-type Ni-gate MOS capacitor before and after the lateral heating treatment. A thin strained Si layer is formed at the Si-SiO_2 interface after the lateral heating treatment.

Chapter 4 High-quality Thin SiO_2 Films Grown by Atomic Layer Deposition

4.1 Introduction

Silicon dioxide is widely used for optical and electronic applications. For example, SiO_2 as gate insulator has been the foundation for the success of integrated circuits in the past decades. Nowadays, oxides with high dielectric constant (high-k) are becoming the mainstream insulators in MOS devices, while SiO_2 is still needed as an interfacial layer between high-k materials and Si substrate in order to obtain superior electrical properties between high-k oxides and silicon [1]. The highest quality SiO_2 is formed by thermal oxidation of silicon at temperatures over 800^0C in dry O_2[2]. The quality of ultrathin thermal oxide grown and processed at high temperature has been extensively investigated in Chapter 3. However, thermal oxide can only be grown on silicon substrates at high temperatures, which limits its applications. For examples, thin-film MOS transistors used for flat-panel displays need gate insulators deposited on thin-film materials; various sensor structures and microelectromechanical systems (*MEMS*) need high-quality SiO_2 film deposited on different substrates other than silicon. Enormous applications can be found if high-quality conformal SiO_2 film can be deposited on non-silicon substrates, e.g. substrates with high aspect-ratio pores and nanostructures. The applications include physical, chemical and biomedical sensors, various MEMS devices, and nanoelectronic devices.

Various techniques have been developed to directly deposit SiO_2 on substrates such as Plasma Enhanced Chemical Vapor Deposition (PECVD), E-beam evaporation, and

Sputtering. However, none of them can produce SiO_2 with quality close to thermal oxide[3-5]. These SiO_2 films are non-stoichiometric with poor quality, exhibit low breakdown fields and many defects. Furthermore, using the above methods one cannot deposit conformal SiO_2 in high-aspect-ratio pores and nanostructures. It is, therefore, very important to find an approach to deposit high-quality conformal SiO_2 films on different substrates and on high aspect-ratio pores and nanostructures.

Atomic layer deposition (ALD) can circumvent these problems because the material is deposited one atomic layer at a time [6-8] through self-limiting surface reactions. Despite its importance, SiO_2 ALD has been difficult to achieve, because silicon does not react with water at a low temperature. In the early stage of ALD studies, catalysts[9] or external energy such as plasma[10] was unavoidable in order to activate the SiO_2 reaction. In the processes, H_2O and H_2O_2 served as oxidant. However, H_2O does not oxidize the silicon precursors effectively and H_2O_2 is corrosive[11]. Recently, ozone was introduced into the reaction process as the oxidant, which is more effective for oxidation of silicon precursors in ALD deposition of SiO_2. Various silanes with different molecular structures, which serve as silicon precursors, were studied for the effectiveness of oxidation, such as alkoxysilanes[9], chlorosilanes[12] and aminosilanes[13-16]. Recently, a self-catalytic 3-steps ALD of SiO_2 using 3-aminopropyltriethoxysilane (APTES), water and ozone was reported[17]. The detailed optical, structural and electrical properties were investigated[18]. It also was reported[19] that TDMAS (tris(dimethylamino)silane $[(CH_3)_2N]_3SiH$), water, and ozone could be used as precursors to grow SiO_2 at low temperatures. In the published researches, there is rare work on thin ALD SiO_2 films under 100 cycles (<5nm). In addition,

most publications dealt with ALD growth and only limited information is available on electrical properties.

In this chapter, we study extensively the physical and electrical properties of thin ALD SiO_2 films under 100 cycles deposited on silicon substrates using Tris(dimethylamino)silane (TDMAS) and ozone at 100^0C, 200^0C and 300^0C. We studied the physical and electrical properties of SiO_2 thin films using ellipsometry measurement of SiO_2 films and electrical measurement of the metal-oxide-semiconductor capacitors.

4.2 Experimental

Thin SiO_2 films were grown by atomic layer deposition (ALD) (Cambridge NanoTech Inc). Tris(dimethylamino)silane (TDMAS) and ozone were chosen as precursors, while ozone was provided by an ozone generator (A2Z Ozone Inc.). TDMAS was heated up to 40^0C to have enough vapor pressure to introduce TDMAS to the reaction chamber. The carrier gas was nitrogen at a flow rate of 10 sccm (standard cubic centimeters per minute). SiO_2 was deposited at 100^0C, 200^0C and 300^0C. Both the substrate susceptor and the wall of the chamber were heated in order to obtain a uniform temperature inside the entire chamber. The pulse time was chosen to meet the saturation requirement of ALD, which means the growth rate does not increase any more with the increase of the pulse time. The deposition parameters used at different temperatures are summarized in table 4.1.

Although it is unnecessary and impossible to introduce pure ozone into ALD chamber, ozone with high concentration is necessary in the deposition of SiO_2, because TDMAS requires strong oxidant. Before loading samples, the pipe connecting ozone generator and ALD chamber has to be purged by ozone to expel residual air. This is accomplished by running 30 cycles of ozone. In each cycle, the purging pulse time was 0.2 seconds, exposure time was 0 second, and pump time was 26 seconds.

Detailed experimental studies of deposition of SiO_2 were carried out with different number of cycles at 100^0C, 200^0C and 300^0C, giving a full view of the ALD growth linearity. At 100^0C, 24, 30, 50, 70, 90 and 150 ALD cycles were deposited; at 200^0C and 300^0C, 10, 20, 30, 50, 100 and 200 ALD cycles were used. For the 300^0C experiment, the temperature at the center of the reaction chamber was 300^0C while the sidewall temperature was 250^0C. This was limited by our ALD system, because the highest sidewall temperature available in our ALD system is 250^0C. Multi-angle Spectroscopic Ellipsometry (*J. A. Woollam* M3000V) was used to obtain the physical thickness and optical constants (refractive index, n, and extinction coefficient, k) of the thin SiO_2 films. These values were determined by fitting the captured data to a pre-built-in standard SiO_2 model.

MOS capacitors were fabricated for the electrical characterization of the atomic layer deposited SiO_2 films at different deposition temperatures. Phosphorus doped n type Si(100) substrates with a resistivity of 1-20 Ω cm were used. The substrates were cleaned using Radio Corporation of America (RCA) cleaning to remove organic and ionic contaminations. The details of RCA cleaning were described in Chapter 2. After RCA cleaning, the

substrates were cleaned using a diluted BOE (buffered oxide etch) solution (Deionized water: BOE = 80 ml: 20 ml), providing an H-terminated surface of the silicon substrates. This is unique because all other researchers used hydroxylated (OH) surfaces of silicon for ALD deposition of SiO_2[14, 17]. After ALD, 1100 Å nickel (Ni) was deposited as gate metal by electron-beam evaporation. The metal was then patterned by photolithography and wet etching. The details of this process were described in Chapter 2. The gate patterns were circles and the diameter was 100μm. Back contact was made by 1000 Å aluminum (Al), which was also deposited by electron-beam evaporation. The samples were annealed at 450^0C in forming gas for 30 min., which created an ohmic contact between Al and the bulk Si, and also passivated the defects in the SiO_2 layer.

The capacitance-voltage (C-V) curves were measured using an Agilent 4284A LCR meter at different frequencies, and the current-voltage (I-V) curves were measured with an Agilent 4155B semiconductor parameter analyzer. Equivalent Oxide Thickness (EOT) and flatband voltage (V_{FB}) were extracted from the 100 KHz C-V curves by UC Berkeley's quantum-mechanical C-V simulator.

4.3 Results and Discussion

4.3.1 Linearity of Atomic Layer Deposition of SiO_2

Figure 4.1 shows the growth linearity of ALD SiO_2 at 100^0C, 200^0C and 300^0C, the *X axis* is the number of ALD cycles, and the *Y axis* is the SiO_2 thin film thickness measured by multi-angle spectroscopic ellipsometry (MSE<5). Each thickness is the average value of three measured points at different locations on each sample. All the depositions at 100^0C,

200^{0}C and 300^{0}C show excellent linearity, which suggests atomic-layer-by-atomic-layer deposition. The deposition rates were extracted by calculating the slope of each straight growth line. At 100^{0}C, the rate was ~0.2Å/cycle; at 200^{0}C, the rate was ~0.7Å/cycle; at 300^{0}C, the rate was ~0.6Å/cycle.

The dependence of growth rate on the substrate temperature could be elucidated by the dissociative chemisorptions of TDMAS on substrate. The molecule structure of silane is $SiH(N(CH_3)_2)_3$. The entire reaction includes Si dangling bonds generation by breaking three dimethylamine groups ($-N(CH_3)_2$) in silane molecules $SiH(N(CH_3)_2)_3$ and the followed Si bonding with O atoms (oxidation)[13-15]. The breaking of first two dimethylamine groups is easy, while the breaking of the third one requires high thermal energy. After breaking the dimethylamine groups, they become gaseous groups ($H-N(CH_3)_2$) and escape from the substrate so that no C and N remain in films. Therefore, creation of Si dangling bonds is strongly dependent on substarte temperature. The higher substrate temperature create more Si dangling bonds, resulting in higher deposition rate. In addition, at 100°C, the ALD SiO_2 growth is still linear, suggesting no physical accumulation of dimethylamine groups inside the film. Impurities in the ALD SiO_2 films were also studied using SIMS by Liu et.al. [20]. According to their SIMS analysis, the impurity levels of the ALD SiO_2 films deposited at 100-350^{0}C are very low. There are ~0% C, ~5% N, and ~15% H in silicon oxide films deposited at 100^{0}C, ~0% C, ~0% N, and ~21% H at 200^{0}C, and ~0% C, ~1% N, and ~15% H at 350^{0}C. Increase of the temperature from 200°C to 300^{0}C does not introduce any further increase of deposition rate. Actually, the deposition rate at 300^{0}C is slightly lower than 200^{0}C, which could be attributed to the

minor unstable supply of O_3 in our ALD system. Based on our dosing tests, the saturation dose of TDMAS is easy to achieve. On the contrast, the dose of O_3 is crucial for the reaction, and a little fluctuation of O_3 can affect the deposition rate.

Plotting extension lines towards *Y axis* in figure 4.1, it is noticeable that the extension lines do not pass through the origin (0 0), but intersect with *Y axis* at 10-15Å. This seems like the atomic layer deposition was executed on top of an initial layer with physical thickness 10-15Å, and evidence needs to be shown that this is not caused by Si substrate regrowth by ozone oxidant at elevated temperature. After etching in buffered oxide etch (BOE), Si substrates were loaded into the ALD reaction chamber, and then only ozone oxidant was introduced into the chamber without the TDMAS source. The pulse and pump time were maintained the same as those in the real SiO_2 deposition process. After several cycles, substrates were taken out of the chamber and the physical thickness of newly grown SiO_2 was measured using multi-angle spectroscopic ellipsometry. The results at different temperatures are listed in Table 4.1. It should be noted that after RCA cleaning and BOE etching, a silicon substrate was thoroughly hydrophobic without any SiO_2, and the ellipsometery measurement produced a baseline reading of 7.49Å. For SiO_2 of <12 Å, The apparent SiO_2 thickness is obtained by subtracting the baseline value from the ellipsometry reading[21]; for SiO_2 of >20 Å, the ellipsometry reading is accurate and no subtraction of the baseline reading is needed (The EOT and ellipsometry reading match very well in our control samples fabricated using high quality thermal SiO_2[22]). All the thickness values listed in table 4.1 are the average value of two measured points at different locations on each sample. The highest SiO_2 regrowth in table 4.2 is the 15 cycles of ozone oxidation at

300^0C, that is only 5.56Å, which is far less than the 10-15Å "initial layer". In the real atomic layer deposition of SiO_2, both TDMAS and ozone are introduced sequentially and chemical reactions are taking place layer by layer, where the ozone thermal oxidation of the Si substrate must be weaker than the ozone oxidation. Thus, the 10-15Å "initial layer" must not be caused by Si substrate oxidation by ozone during atomic layer deposition. The reason for the fast initial growth during the beginning 10 ALD cycles might be the non-uniform pile-up of precursor molecules on an H-terminated surface and the followed non-uniform nucleation instead of forming uniform chemical coverage [23, 24].

4.3.2 Electrical Properties of Ultrathin ALD SiO_2 Films

Comparing to other techniques, the thermal oxidation provides lowest gate leakage current and largest breakdown electrical field. For SiO_2 dielectric thinner than 3-4 nm, the leakage current mechanism is mainly quantum-mechanical tunneling (direct tunneling)[25]. The direct tunneling current depends exponentially on SiO_2 thickness, every 0.2nm increase of the SiO_2 thickness results in one order of magnitude reduction of the direct tunneling current[26-28].

Metal-oxide-Semiconductor (MOS) capacitors were fabricated on the 100^0C ALD SiO_2 samples to test their electrical properties. 100 KHz capacitance-voltage (C-V) and current-voltage (I-V) curves are shown in figure 4.2, where the three curves are obtained from the MOS capacitors using 50, 70 and 90 cycles of ALD SiO_2 respectively. Each one of the curves is the typical curve of 10-15 measured devices. The electrical curves of ALD SiO_2 of 24 and 30 cycles are not shown because of deformed C-V curves caused by large leakage

current[27]. From the 100 KHz C-V curve, we extracted the EOT of 50 cycles SiO_2 to be 2.34 nm, and the flatband voltage (V_{FB}) is 0.77V. The corresponding gate leakage current of the same device at $V=V_{FB}+1V$ is 9×10^{-2} A/cm^2, which matches well with the reported gate leakage current of thermally grown SiO_2 [26-28]. The EOT of the 70 cycles ALD SiO_2 is 2.68 nm, which is 0.34 nm thicker than the 50 cycles SiO_2, and the corresponding gate leakage current at $V=V_{FB}+1V$ is 5×10^{-3} A/cm^2 (V_{FB}=0.71V), which is 1.5 order of magnitude lower than the 50 cycles SiO_2. Similar to the thermal SiO_2, when thinner than 3 nm, the direct tunneling current of ALD SiO_2 depends exponentially on SiO_2 thickness, every 0.2 nm thickness increase corresponds to 1 order of magnitude tunneling leakage current reduction. This is further verified by results of 90 cycles ALD SiO_2.For EOT of 2.89 nm, the gate leakage current at $V=V_{FB}+1V$ is in the 10^{-5} order.

Figure 4.3 and 4.4 show the C-V and I-V curves of MOS capacitors with ALD SiO_2 deposited at 200 and 300^{0}C respectively. Similar results are exhibited here: the gate leakage current at $V=V_{FB}+1V$ is comparable with that of thermally grown SiO_2, and the leakage current depends exponentially on SiO_2 thickness. The only exception is the 30 cycles of ALD SiO_2 at 200^{0}C, of which the EOT is 3.2 nm, and the gate leakage current at $V=V_{FB}+1V$ is larger than expectation (4×10^{-4}A/cm^2). Since this larger leakage current is the only case among many data, it could be attributed to mal-fabrication, e.g. ion contamination.

In order to further illustrate the quality of the deposited ultrathin ALD SiO_2 films, we carried out measurement of frequency dispersion and hysteresis behavior of the C-V curves,

and the results are added as figure 4.5. Figure 4.5(a) is the frequency dispersion of C-V curves of a MOS capacitor using ultrathin ALD SiO_2 (EOT 2.68nm) deposited at 100^0C as gate dielectric. C-V curves at 10 KHz, 100 KHz and 1 MHz overlap with each other, which implying good interface quality. Figure 4.5(b) shows the hysteresis behavior of 100 KHz C-V curve of the same capacitor. In figure 4.5(b), the solid curve was measured from depletion to accumulation, and the dash curve was measured from accumulation to depletion. The two curves overlap with each other, which suggests the slow trap charges in the SiO_2 film is negligible.

The frequency dispersion and hysteresis of C-V curves of the MOS capacitor using ultrathin ALD SiO_2 deposited at 200^0C (EOT 2.41nm) are shown in figure 4.5(c) and 4.5(d). These curves are similar with the 100^0C ALD SiO_2 results, which corresponds to their similar electrical properties illustrated above. The results of 300^0C ALD SiO_2 are not shown here because they are similar to results at 100^0C and 200^0C. The interfacial quality and impurity levels of the ALD SiO_2 films deposited at 100°C, 200^0C, and 300^0C are all very good in this thickness region (<3.5 nm).

In contrast to the ALD, any other techniques, such as PECVD and sputtering, cannot deposit SiO_2 with gate leakage current comparable to that of thermally grown SiO_2 [4, 29]. The two-step ALD deposition of SiO_2 using TDMAS and ozone provides a way to achieve dielectric SiO_2 with excellent gate leakage current comparable with thermally grown SiO_2 when the thickness is less than 3.5nm. The breakdown electrical fields of the ALD SiO_2

are not discussed in this thickness range, since no obvious electrical breakdown occurs in ultrathin dielectric layers. The electrical breakdown property will be discussed in part 4.3.4.

4.3.3 Difference Between Physical and Equivalent Oxide Thicknesses (EOT)

Figures 4.6, 4.7, and 4.8 show High frequency (100 KHz) capacitance-voltage (C-V) curve and Current-Voltage (I-V) curve of MOS capacitors using ALD SiO_2 as gate dielectrics deposited at 100^0C, 200^0C, and 300^0C. The Equivalent Oxide Thickness (EOT) of ALD SiO_2 grown at different temperatures was compared with the physical thickness measured by multi-angle spectroscopic ellipsometry. The comparison was conducted for all cycle numbers, except for 24, 30 cycles at 100^0C, and 10 cycles at 200^0C, 300^0C, of which the C-V curves are deformed due to large leakage current. A distinct mismatch exists between EOT and physical thickness obtained by ellipsometry, the EOT is always smaller than the physical thickness, and the detailed information is shown in table 4.3. The mismatch in percentage is defined as: Mismatch (%) = (Ellipsometry thickness-EOT)/Ellipsometry thickness×100%.

Generally speaking, as the cycle number increases, the mismatch between EOT and physical thickness increases, too, although this is not a strict rule without exceptions. With 50 cycles at 100^0C, the physical thickness is 2.42 nm, and the EOT is 2.34 nm, which only exhibits 3.3% mismatch. This percentage increases to 8.2% for 70 cycles, 14.2% for 90 cycles, and then slightly changes back to 10.7% for 150 cycles. At 200^0C, the variation range of mismatch is huge, which starts from 12.4% for 20 cycles, to 48.1% for 200 cycles. At 300^0C, the smallest mismatch, from the 20-cycle ALD, is already 18%, which is even

larger than peak value (14.2%) of the mismatch at 100^0C. The largest mismatch at 300^0C occurred at the 200-cycle ALD, which is 42.4%. At all three deposition temperatures, it is clear that mismatch increases with cycle number. The only exceptional data are those for 30 cycles at 200^0C, which only show 7.8% mismatch. Since this device also showed gate leakage current larger than the expected value (see Part 4.3.2), which might be caused by mal-fabrication such as ion contamination, the exception here could also be attributed to defects during fabrication.

The dependence of mismatch between EOT and physical thickness on deposition temperature was also evaluated from Table 4.3 based on SiO_2 thin films of similar physical thicknesses. For examples, the SiO_2 thin film of 2.42 nm physical thickness obtained at 100^0C corresponds to 3.3% mismatch, while that of 2.44 nm at 300^0C corresponds to 18% mismatch, which is significantly higher. The SiO_2 thin film of 2.92 nm obtained at 100^0C exhibits 8.2% mismatch, while that of 2.75 nm at 200^0C exhibits 12.4% mismatch. The SiO_2 thin film of 3.37 nm obtained at 100^0C corresponds to 14.2% mismatch, and that of 3.11 nm at 300^0C corresponds to 22.5% mismatch (The films obtained by ALD for 30 cycles at 200^0C is not considered here because of the possible mal-fabrication). For physical thickness of 4-5 nm, the mismatchs of SiO_2 thin films deposited at 100°C, 200°C and 300°C are 10.7%, 26.6% and 20.2% respectively. From the above analysis, it is concluded that for similar physical thickness, thin SiO_2 films deposited at 100^0C exhibits the smallest mismatch between EOT and physical thickness, and that is significantly increased when the deposition temperature increased from 100^0C to 300^0C.

Figure 4.9(a) and 4.9(b) are the frequency dispersion and hysteresis behavior of C-V curves of MOS capacitor using 4.6nm ALD SiO_2 (EOT 4.1nm) deposited at 100^0C as gate dielectric. There is no frequency dispersion among the C-V curves obtained at 10 KHz, 100 KHz and 1 MHz, neither obvious hysteresis behavior. Careful comparison of figure 4.9(b) to figure 4.5(b) and figure 4.5(d) shows that, in figure 4.5(b) and 4.5(d), the solid curve and the dash curve overlap with each other in the entire voltage range, while in figure 4.9(b), we can barely distinguish the dash curve from the solid curve near the V_{FB} region. However, this is just a subtle phenomenon. The frequency dispersion and hysteresis behavior imply good interface quality and negligible slow trap charges in the oxide layer. In the contrast, ALD SiO_2 deposited at 200^0C with similar physical thickness exhibits different behaviors. In figure 4.9(c), the MOS capacitor using 4.85nm ALD SiO_2 (EOT 3.56nm) deposited at 200^0C as gate dielectric shows obvious C-V frequency dispersion, especially near the V_{FB} region. The hysteresis behavior in figure 4.9(d) is different from the previous results in the sense that the V_{FB} shifts towards the negative direction when the voltage is scanned from accumulation to depletion. The shift of V_{FB} is caused by positive slow trap charges in the oxide layer[30], which might be caused by impurity accumulation:

$$\Delta V'_{FB} = -\frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx$$

ALD SiO_2 of >3.5nm deposited at 300^0C exhibited the similar C-V frequency dispersion and hysteresis behavior, which are not included here. The interfacial quality of the ALD SiO_2 films deposited at 200^0C and 300^0C are not very good in this thickness region (>3.5nm).

The mismatch phenomena suggest that the ALD SiO_2 is electrically thinner than its physical thickness. Therefore, it is reasonable to assume that the dielectric constant (k value) of the deposited films is higher than its theoretical value of ideal SiO_2. Illustration is needed for whether the mismatch between EOT and physical thickness could be attributed to the impurity in the films. As discussed in Section 4.3.1, Liu et.al. analyzed the impurity levels in the ALD SiO_2 thick films (>15 nm) using SIMS [20]. According to their results, for films deposited from 100°C to 300°C, the C impurity is very low and negligible (<0.2%), the N impurity is less than 3.6%, and only H concentration is higher (15-21%). As shown in Table 4.3, the mismatch of our thicker silicon oxide samples (>5 nm) are 28%-48%, which is much larger than the C and N imputirty concentrations. It is unlikely that C and N impurities could cause the mismatch. Regarding H impurity in samples, H is the lightest atoms and H-doped SiO_2 should result in lower density, causing lower dielectric constant or lower k value, which is opposite to our observation of mismatch. Therefore, the mismatch is not caused by impurities.

In order to understand the mismatch clearly, we describe the phenomena based on ALD reaction mechanism. The ALD reaction includes two steps: (1) Si dangling bonds generation by breaking three dimethylamine groups ($-N(CH_3)_2$) in silane molecules $SiH(N(CH_3)_2)_3$ and (2) Si bonding to O atoms (oxidation). The breaking of first two dimethylamine groups is easy, while the breaking of the third one requires high thermal energy. After breaking the dimethylamine groups, they become gaseous groups ($H-N(CH_3)_2$) and escape from the substrate so that no C and N remain in films. Therefore, creation of Si dangling bonds is strongly dependent on substarte temperature. It is well

known that oxidation of Si in O_2 at temperatures below 300°C is negligible. It is expected that oxidation of Si in O_3 may be better than oxidation in O_2, but is still slow at temperatures below 300°C. In table 4.2, at 5 cycles, the thickness of the SiO_2 grown by thermal O_3 oxidation only increases less than 1Å by increasing the temperature from 100^0C to 300^0C, so we believe that the increase in temperature from 100^0C to 300^0C does not increase the oxidation rate. Therefore, the rate for Si bonding to O atoms (or oxidation rate) is very low from 100^0C to 300^0C, which is the limiting factor for the entire reaction. As a result, at 100^0C, Si dangling bonds generation rate is very low, which is close to the rate for Si bonding to O atoms (oxidation rate), so that the silicon oxide film is more close to stoicheometry. Our experiments also showed that at 100°C, silicon oxide with less mismatch can be deposited. At temperatures >200°C, Si dangling bonds generation rate is much higher due to higher thermal energy so that not all Si dangling bonds are connected to O atoms because of low oxidation rate, but connected to Si themselves or H atoms, resulting in Si-rich silicon oxide. Our experiments also showed that at temperatures >200°C, the deposition rate of SiO_2 is much higher, but the mismatch is also larger. Because silicon has a dielectric constant much higher than SiO_2 (k=11.9 for Si), the silicon-rich SiO_2 thin film should have higher dielectric constant value than thermal SiO_2 so that the EOT of ALD Si-rich SiO_2 film is less than its physical thickness observed using ellipsometry. Therefore the mismatch is caused by non-stoicheometry (Si-rich) of SiO_2 and is larger at higher deposition temperatures.

4.3.4 Breakdown of ALD SiO_2

The applied gate voltage in the I-V characterization was extended until the breakdown of the measured MOS capacitors occurs, and the breakdown voltage (V_{BD}) was recorded for each device (See Figures 4.2, 4.4, 4.6-4.8). At each deposition temperature and cycle number, more than 10 devices were measured in order to achieve statistic results. Ultrathin ALD SiO_2 films with less cycle numbers were not included because there is no obvious electrical breakdown. Since there is a mismatch between the EOT and the physical thickness (see Part 4.3.3), the breakdown electrical fields were evaluated separately based on both of them. The breakdown electrical field based on EOT was calculated as V_{BD}/EOT, where the EOT of each device was extracted from the 100 KHz C-V curve. The breakdown electrical field based on physical thickness was calculated as V_{BD}/ellipsometry thickness, where the ellipsometry thickness was the average of 3 measured points. EOT is a key parameter for gate dielectrics of thin film MOS field-effect transistors (MOSFETs). V_{BD} divided by EOT must be considered when ALD SiO_2 is to be used as gate dielectric for MOS transistors. Because our ALD SiO_2 is Si-rich, it exhibits higher permittivity value, similar to that of high-k gate oxides. V_{BD}/EOT can gauge the quality of SiO_2 as gate dielectric for thin-film MOSFETs because physical thickness is not important in this case. The statistic results of the ALD SiO_2 breakdown electrical fields are shown in details in table 4.4, the numbers in the table are the quantities of MOS capacitors which have breakdown electrical fields in the corresponding range.

The average breakdown electrical field can be used to illustrate the electrical strength of the ALD SiO_2. On the basis of our results, the average breakdown E-field shows thickness

dependence. At all three deposition temperatures, ALD SiO_2 with less cycle numbers exhibit higher breakdown E-fields. As the cycle numbers increase, the breakdown E-fields reduce. This trend is in an agreement with the mismatch between EOT and physical thickness, that thinner films exhibit both smaller mismatch and better electrical strength. We believe that the underlying mechanism for both of the phenomena is the composition and structure of the deposited films: the ALD SiO_2 films are silicon-rich due to insufficient oxidation of silane. The high concentration of silicon results in a high dielectric constant, the electrical strength could be degraded because of the non-stoichiometry of ALD SiO_2. Additionally, thermal SiO_2 grown above 800^0C also shows an inverse proportion of breakdown E-field to the oxide thickness similar to our results[31].

The breakdown E-field of thermal SiO_2 grown above 800^0C has been extensively reported before in literatures. The thermal SiO_2 has a typical breakdown E-field of ~10 MV/cm [31-33]. Based on EOT, the highest breakdown E-Fields of the ALD SiO_2 are 12.2 MV/cm, 9.9 MV/cm and 14.7 MV/cm at 100^0C, 200^0C and 300^0C respectively. These data points are comparable with the thermal SiO_2. As the cycle numbers increase, the breakdown E-Fields slightly decrease. Nevertheless, the electrical strength of material should be more accurately evaluated using the physical thickness based breakdown E-Fields. From this point of view, the 90-cycle deposition at 100^0C and the 30-cycle deposition at 300^0C still possess breakdown E-Fields higher than 10 MV/cm, that is 10.7 MV/cm and 11.5 MV/cm respectively. This suggests that SiO_2 deposited by ALD has the possibility to achieve electrical strength comparable to high-quality thermally grown SiO_2 at the thickness range important to transistors (<3.5nm). Other deposition techniques of SiO_2, such as PECVD,

sputtering, and E-beam evaporation, produce SiO_2 thin films with much lower breakdown E-Fields [34-36], which limited their applications.

4.4 Conclusion

High quality ALD SiO_2 thin films were grown using TDMAS and ozone at different temperatures. Excellent linearity for growth was observed, suggesting atomic layer by atomic layer growth was achieved. The growth rate increased at higher temperatures. When thickness <3.5 nm based on EOT, the ALD SiO_2 has gate leakage current density comparable to that of thermal silicon oxide grown at temperatures above 800^0C. The frequency dispersion and hysteresis behavior of the C-V curves of the ALD SiO_2 films deposited at 100°C, 200^0C, and 300^0C are all very small in the thickness region of <3.5 nm, suggesting excellent interfacial quality. Based on analysis of mismatch between the films' EOT and their physical thicknesses, the ALD SiO_2 thin films are likely to be silicon-rich in composition. At the deposition temperature of 100°C and for thickness <3.5 nm, which is important to thin-film MOS transistors, the EOT-based breakdown electrical fields (~10MV/m) of ALD SiO_2 are nearly as good as that of thermal silicon oxide, and the physical thickness-based breakdown electric-fields (~8MV/cm) are slightly worse than that of thermal silicon oxide, although the thin films contain more H impurity than thermal silicon oxide. At deposition temperatures of 200°C and 300°C, the EOT-based breakdown e-fields (9-10MV/cm) of ALD SiO_2 are close to that of the thermal SiO_2 and the physical thickness-based breakdown e-fields (5-8MV/cm) are worse than that of thermal SiO_2. At all deposition temperatures, the ultrathin ALD SiO_2 (<3.5nm) has both excellent EOT- and physical thickness-based breakdown e-fields (~10MV/cm), which are almost comparable

to that of thermal silicon oxide. The appealing electrical properties of thin ALD SiO_2 (<3.5 nm) enable its potential applications as high-quality gate insulators for thin-film MOS transistors, and insulators for sensor structures and nanostructures on non-silicon substrates.

Table 4.1: ALD programs for deposition of SiO_2 using TDMAS and ozone at 100^0C, 200^0C and 300^0C.

Chamber temperature = 100°C			
Precursor	Pulse time (sec)	Exposure time(sec)	Pump time (sec)
TDMAS	0.03	28	30
Ozone	0.4	30	23
Chamber temperature = 200°C			
TDMAS	0.03	28	23
Ozone	0.4	15	23
Susceptor temperature = 300°C, wall temperature = 250°C			
TDMAS	0.03	28	20
Ozone	0.4	7	20

Table 4.2: Ozone oxidation of Si substrates with the TDMAS source closed using the same experimental parameters as those in the real ALD SiO_2 process.

Temperature	Number of ALD Cycles		
	5	20	30
100^oC	3.95Å	4.11Å	3.97Å
	Number of ALD cycles		
Temperature	5	10	15
200^oC	4.61Å	4.81Å	5.06Å
300^oC	4.63Å	4.80Å	5.56Å

Table 4.3: Mismatch between the physical thickness of ALD SiO2 measured by multi-angle spectroscopic ellipsometry and the EOT. The percentage of mismatch is defined as (Ellipsometry thickness-EOT)/Ellipsometry thickness×100%.

Temperature	Cycle Number	Ellipsometry (nm)	EOT (nm)	Mismatch (%)
100^0C	50	2.42	2.34	3.3%
	70	2.92	2.68	8.2%
	90	3.37	2.89	14.2%
	150	4.59	4.1	10.7%
200^0C	20	2.75	2.41	12.4%
	30	3.47	3.2	7.8%
	50	4.85	3.56	26.6%
	100	8.45	5.09	39.8%
	200	15.4	8	48.1%
300^0C	20	2.44	2	18%
	30	3.11	2.41	22.5%
	50	4.19	3.35	20.2%
	100	6.96	5	28.3%
	200	12.5	7.2	42.4%

Table 4.4: Breakdown electrical fields of ALD SiO2 deposited at 100^0C, 200^0C and 300^0C respectively. The numbers are the quantities of MOS capacitors which have breakdown electrical fields in the corresponding range. The electrical fields based on EOT and physical thickness are calculated separately because of the mismatch between EOT and physical thickness.

(a) ALD SiO_2 deposited at 100^0C

E-Field based on EOT (MV/cm)	**9~10**	**10~11**	**11~12**	**12~13**	**13~14**	**Average Breakdown E-field**
90 cycles (2.89nm)	1		1	8	1	12.2 MV/cm
150 cycles (4.1nm)	7	2				9.5 MV/cm
E-Field based on Ellipsometry (MV/cm)	**8~9**	**9~10**	**10~11**	**11~12**	**9~10**	**Average Breakdown E-field**
90 cycles (3.37nm)	1	1	3	6		10.7 MV/cm
150 cycles (4.6nm)	9					8.5 MV/cm

(b) ALD SiO_2 deposited at 200^0C

E-Field based on EOT (MV/cm)	**5~6**	**6~7**	**8~9**	**9~10**	**10~11**	**11~12**	**Average Breakdown E-field**
50 cycles (3.56nm)				6	5		9.9 MV/cm
100 cycles (5.09nm)			4	7	1		9.1 MV/cm
200 cycles (8nm)	2	1	1		2	5	9.7 MV/cm
E-Field based on Ellipsometry (MV/cm)	**2~3**	**3~4**	**4~5**	**5~6**	**6~7**	**7~8**	**Average Breakdown E-field**
50 cycles (4.85nm)						11	7.5 MV/cm
100 cycles (8.45nm)			1	11			5.5 MV/cm
200 cycles (15.4nm)	1	2	1	2	5		5.2 MV/cm

(c) ALD SiO2 deposited at 300^0C

E-Field based on EOT (MV/cm)	**7~9**	**9~10**	**10~11**	**11~12**	**12~13**	**13~14**	**>14**	**Average Breakdown E-field**
30 cycles (2.41nm)					1	2	8	14.7 MV/cm
50 cycles (3.35nm)		1	4	7				10.8 MV/cm
100 cycles (5nm)	4	6	3					9.1 MV/cm
200 cycles (7.2nm)			2	8	2			11.4 MV/cm
E-Field based on Ellipsometry (MV/cm)	**<6**	**6~7**	**7~8**	**8~9**	**9~10**	**10~11**	**>11**	**Average Breakdown E-field**
30 cycles (3.11nm)						2	9	11.5 MV/cm
50 cycles (4.19nm)			1	6	5			8.8 MV/cm
100 cycles (6.97nm)	4	7	2					6.3 MV/cm
200 cycles (12.5nm)		11	1					6.6 MV/cm

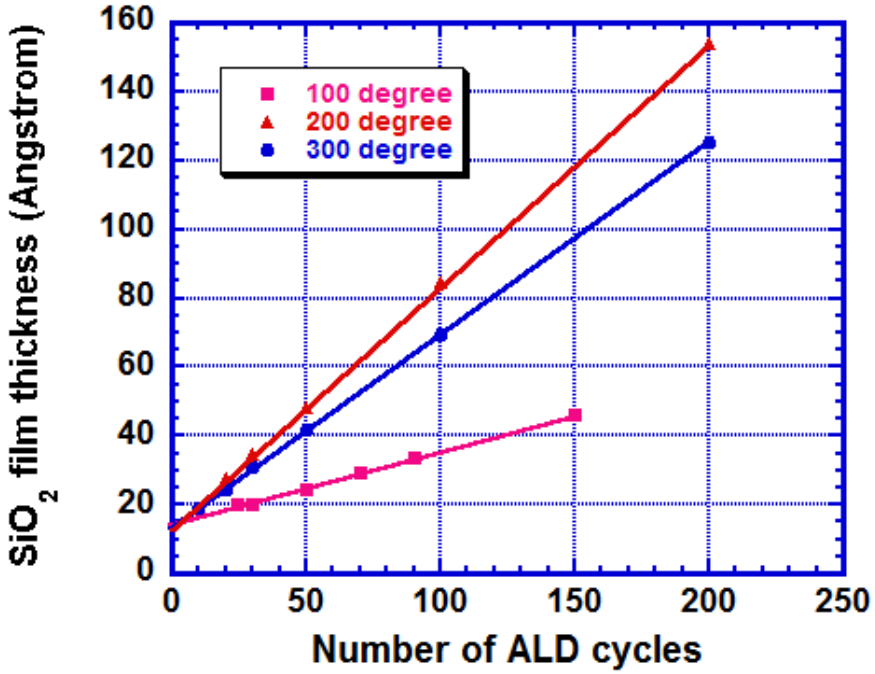


Fig 4.1. Linearity of the atomic layer deposition of SiO_2 at 100^0C, 200^0C and 300^0C. Film thickness was obtained by spectroscopic ellipsometry. At 100^0C, 24, 30, 50, 70, 90 and 150 cycles were carried out; at 200^0C, 10, 20, 30, 50, 100, 200 cycles were carried out; at 300^0C, 10, 20, 30, 50, 100, 200 cycles were carried out.

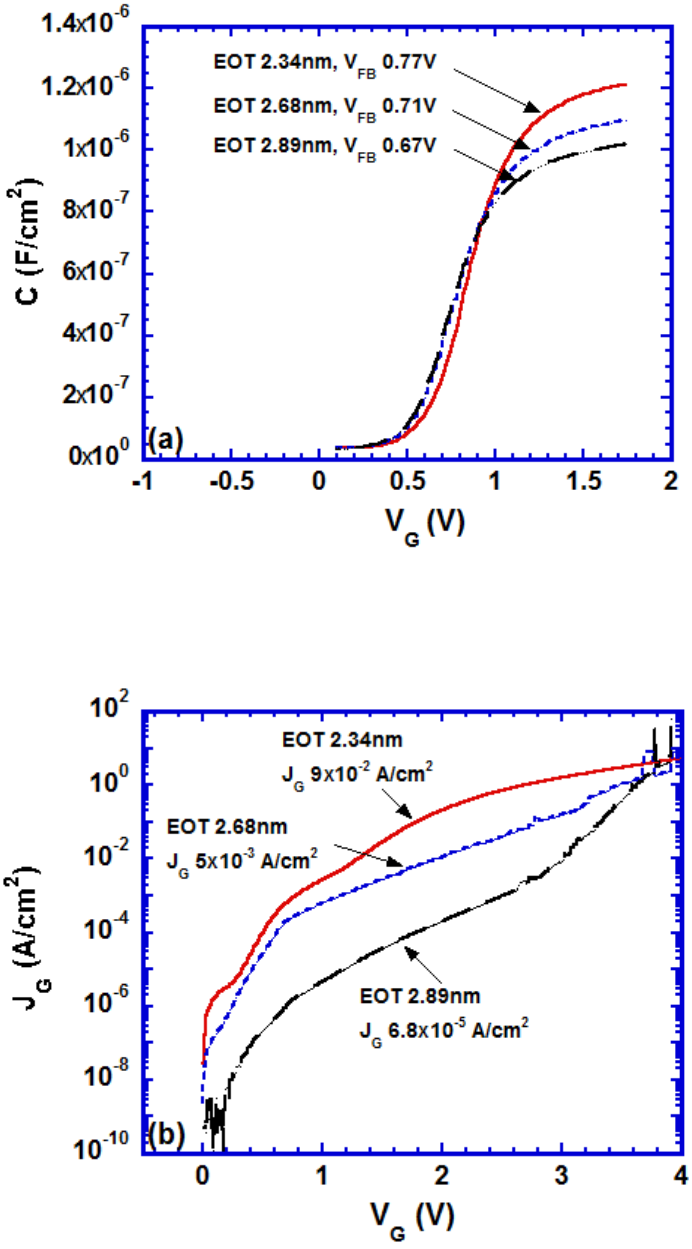


Fig 4.2. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curves and (b) Current-Voltage (I-V) curves of MOS capacitors using ALD SiO_2 at 100^0C as dielectric. The SiO_2 thin films were deposited for 50, 70 and 90 cycles, and correspond to EOT 2.34 nm, 2.68 nm and 2.89 nm respectively. Each one of the curves is a typical representative of 10-15 measured devices. The gate patterns were circles and the diameter was 100μm.

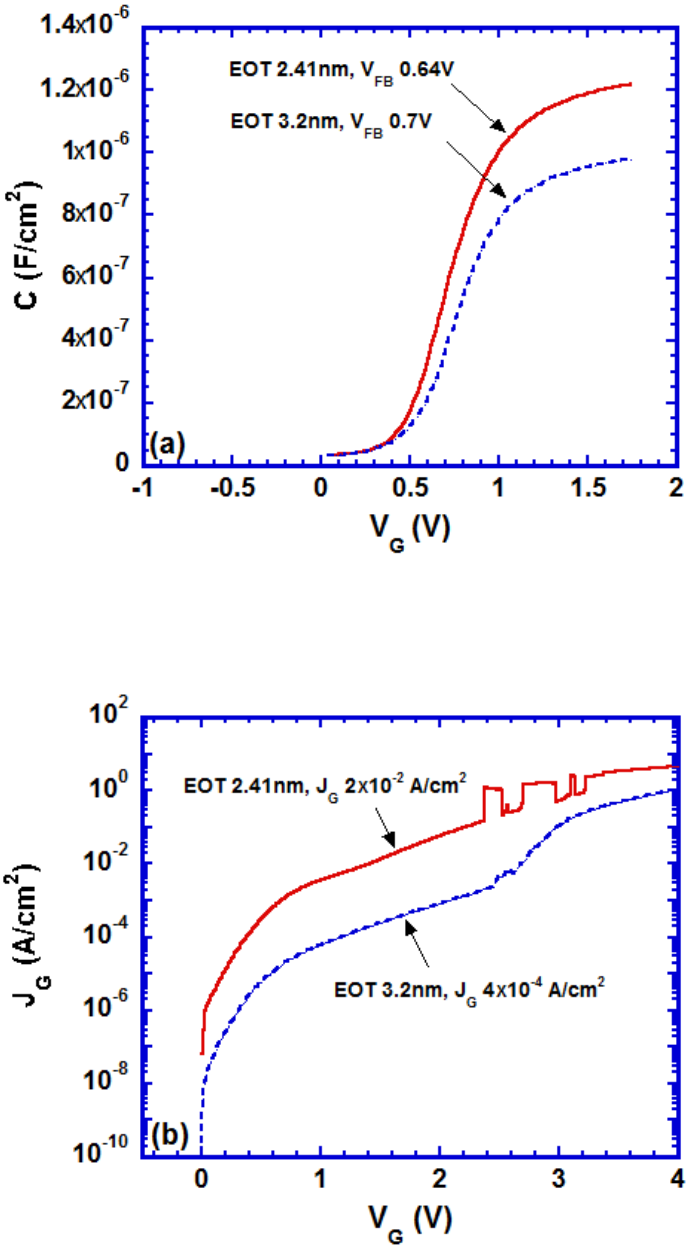


Fig 4.3. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curves and (b) Current-Voltage (I-V) curves of MOS capacitors using ALD SiO_2 at 200^0C as gate dielectric. The SiO2 thin films were deposited for 20 and 30 cycles, and correspond to EOT 2.41 nm and 3.2 nm respectively. Each one of the curves is a typical representative of 10-15 measured devices.

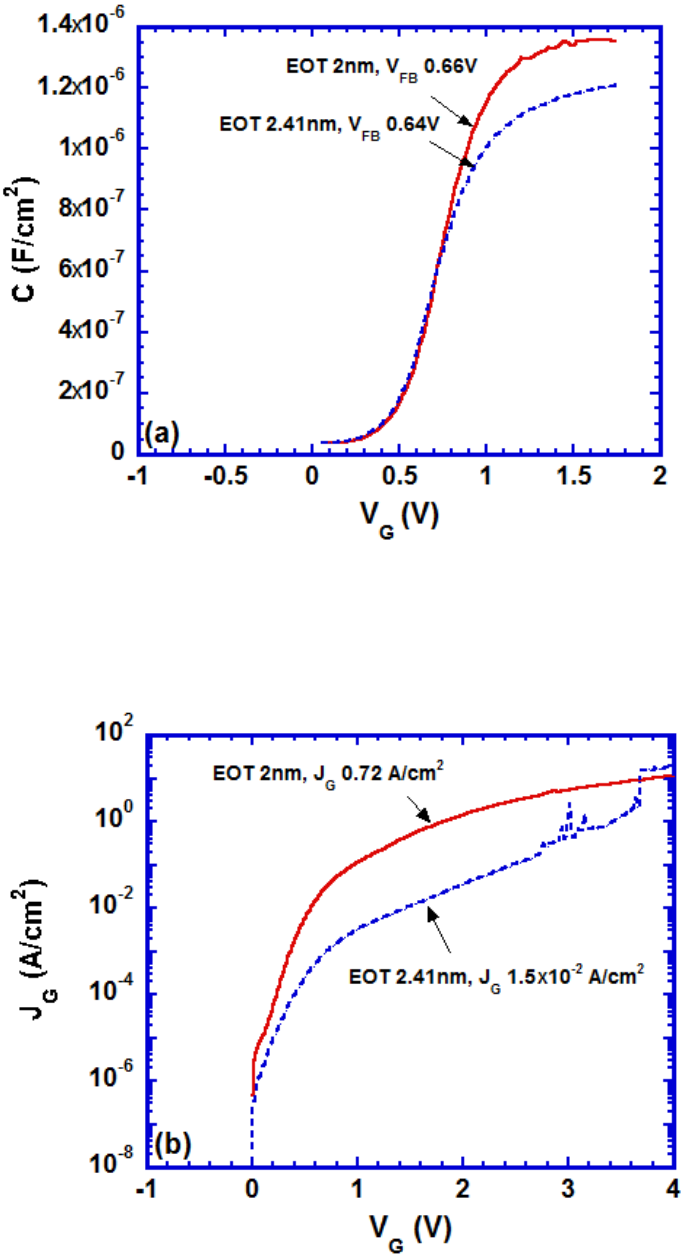


Fig 4.4. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curves and (b) Current-Voltage (I-V) curves of MOS capacitors using ALD SiO_2 at 300^0C as gate dielectric. The SiO2 thin films were deposited for 20 and 30 cycles, and correspond to EOT 2 nm and 2.41 nm respectively. Each one of the curves is a typical representative of 10-15 measured devices.

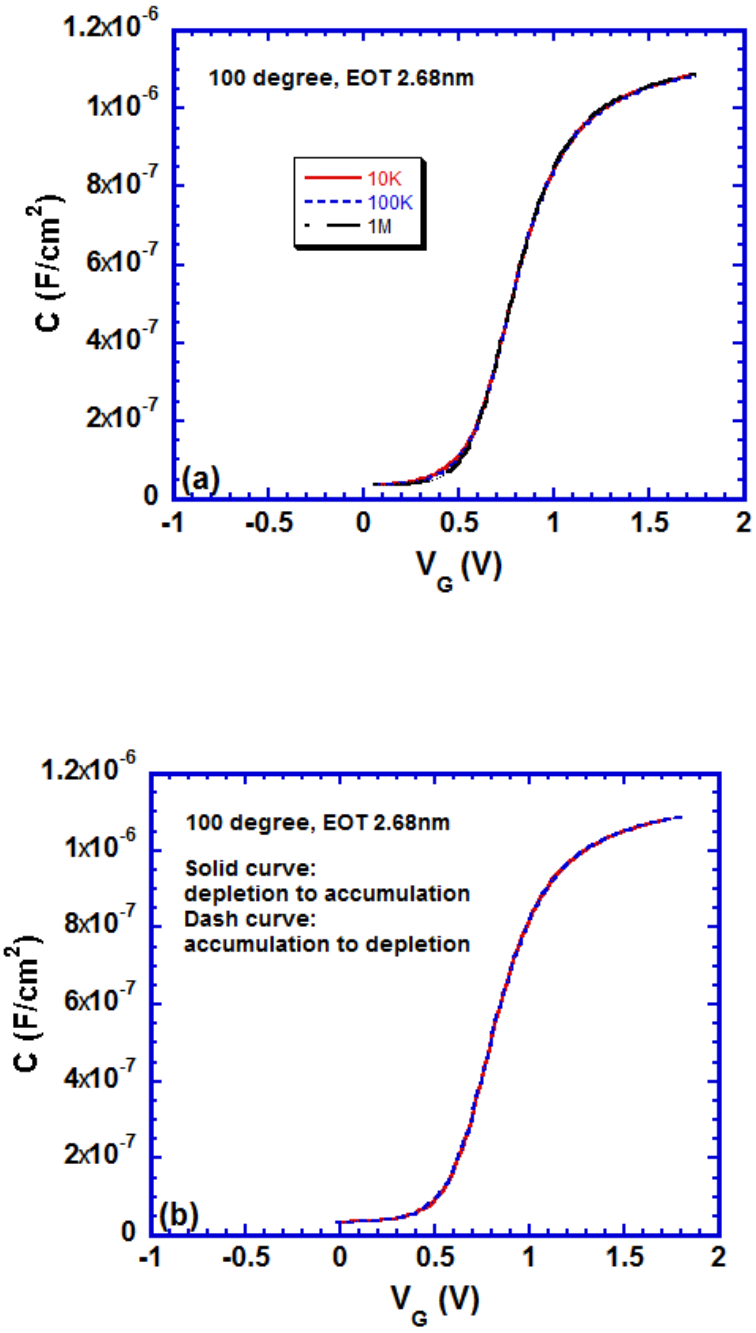


Fig 4.5. (a) Frequency dispersion (10KHz, 100KHz, 1MHz) of C-V curves of MOS capacitor using ultrathin ALD SiO_2 deposited at 100^0C as gate dielectric. (b) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in figure 5(a).

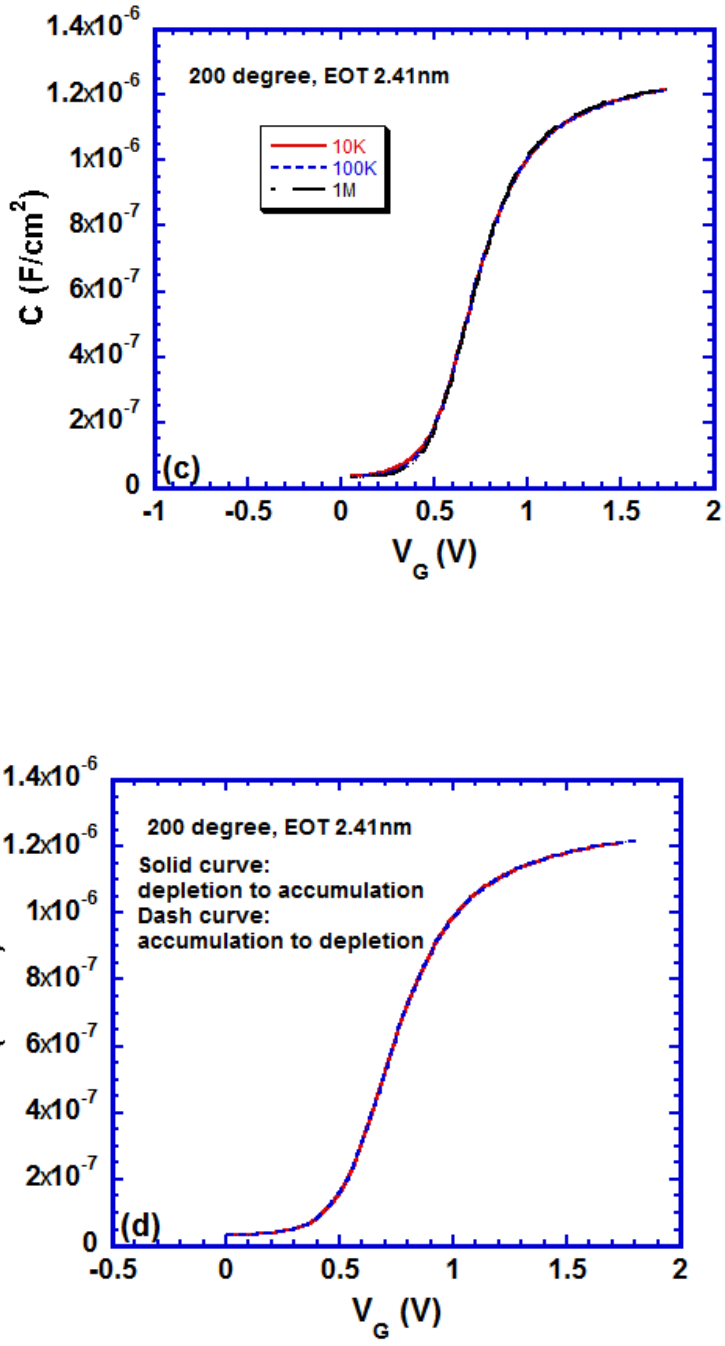


Fig 4.5. (c) Frequency dispersion of C-V curves of MOS capacitor using ultrathin ALD SiO_2 deposited at 200^0C as gate dielectric. (d) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in figure 5(c).

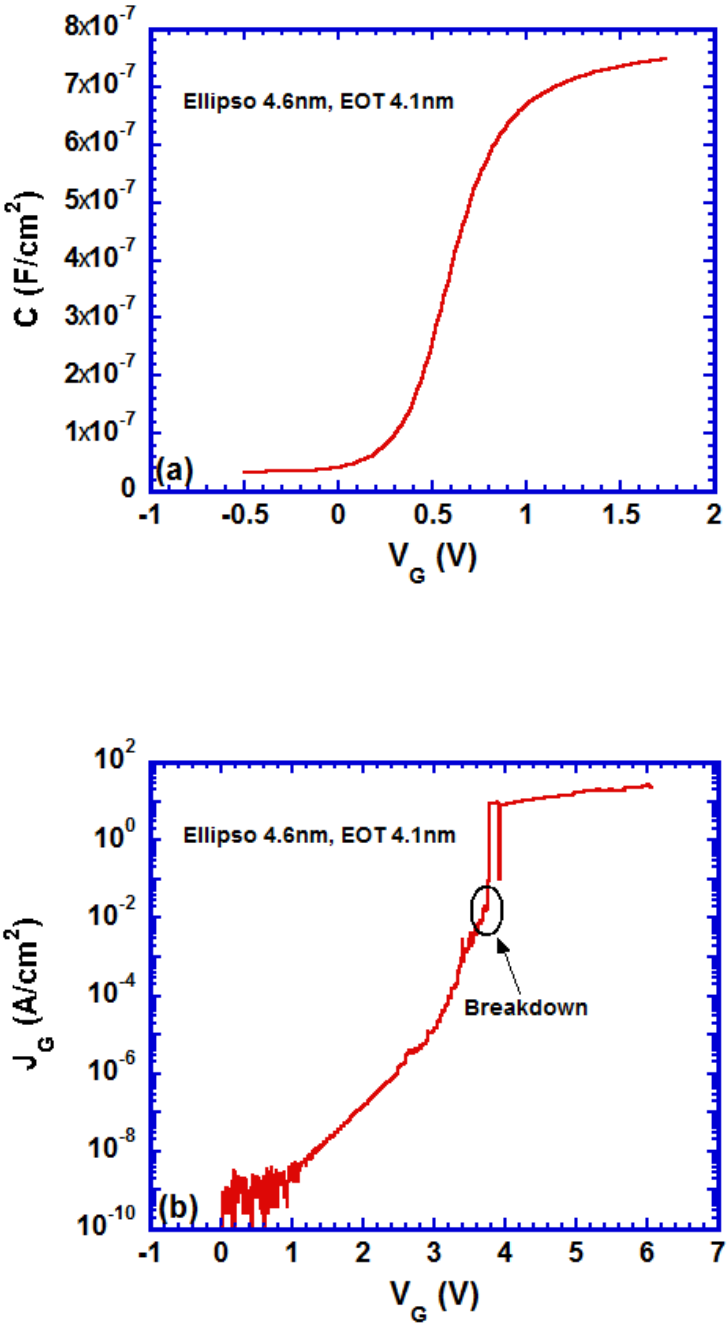


Fig 4.6. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curve and (b) Current-Voltage (I-V) curve of MOS capacitor with ALD SiO_2 at 100^0C as gate dielectric. The SiO2 thin films were deposited for 150 cycles. The curve is the typical representative of 10-15 measured devices. The electrical breakdown of the device is marked on the I-V curve.

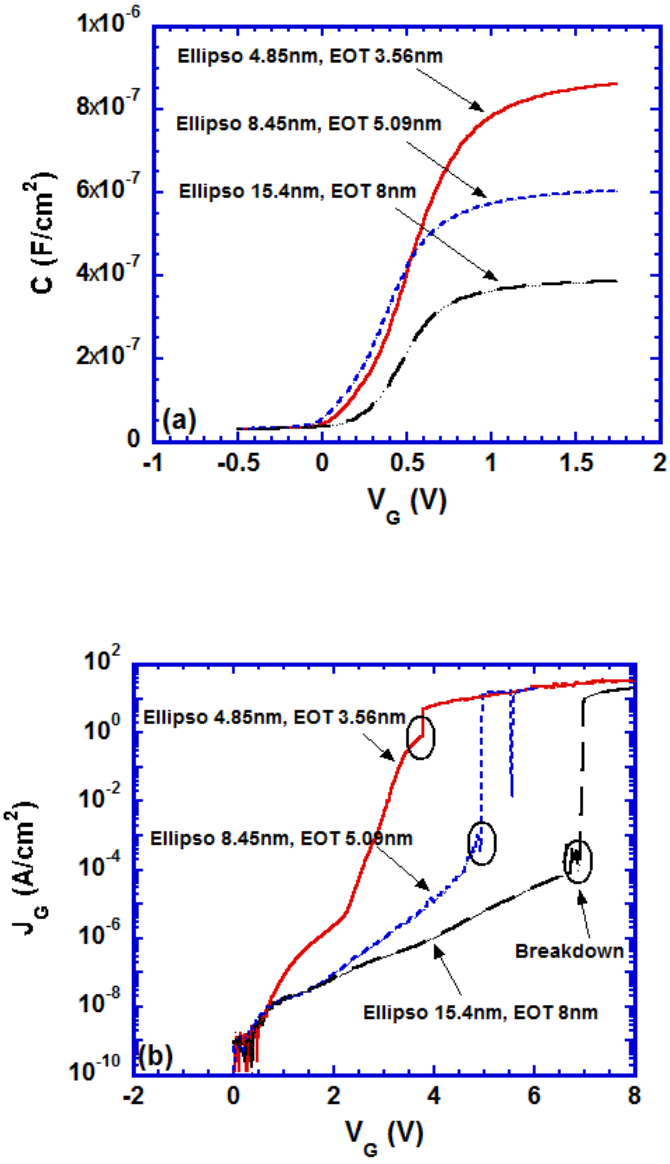


Fig 4.7. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curves and (b) Current-Voltage (I-V) curves of MOS capacitors with ALD SiO_2 at 200^0C as gate dielectric. The SiO2 thin films were deposited for 50, 100 and 200 cycles respectively. Each curve is a typical representative of 10-15 measured devices. The electrical breakdown of the device is marked on the I-V curve.

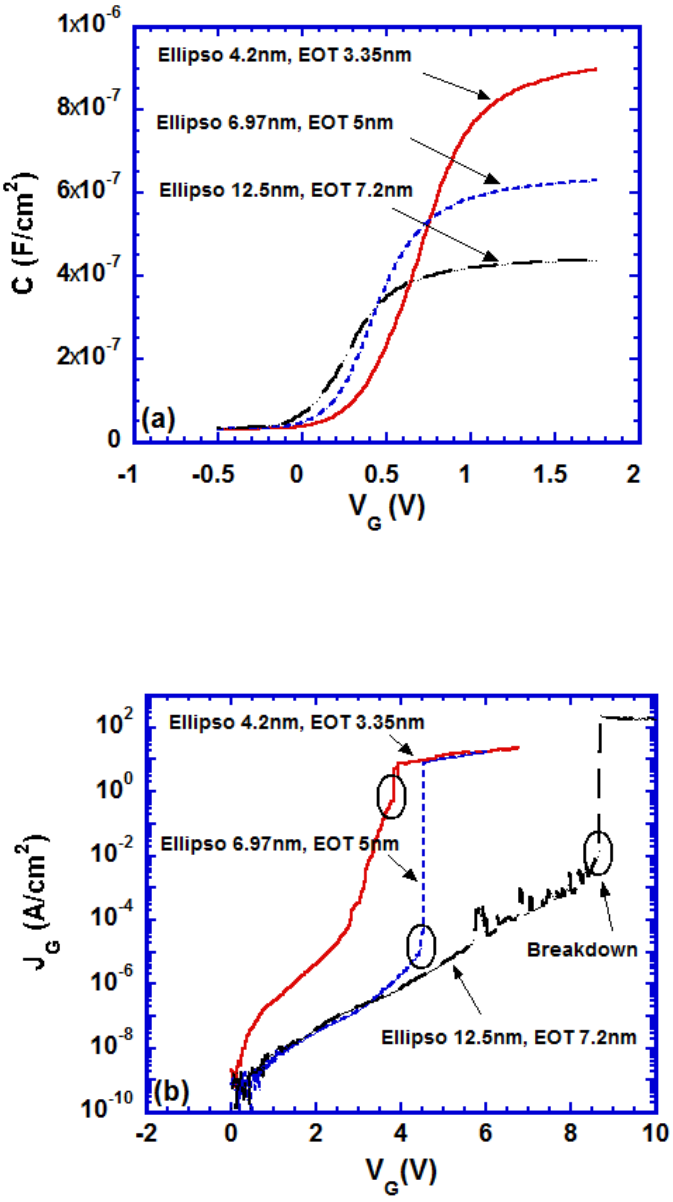


Fig 4.8. (a) High frequency (100 KHz) Capacitance-Voltage (C-V) curves and (b) Current-Voltage (I-V) curves of MOS capacitors with ALD SiO_2 at 300^0C as gate dielectric. The SiO2 thin films were deposited for 50, 100 and 200 cycles respectively. Each curve is a typical representative of 10-15 measured devices. The electrical breakdown of the device is marked on the I-V curve.

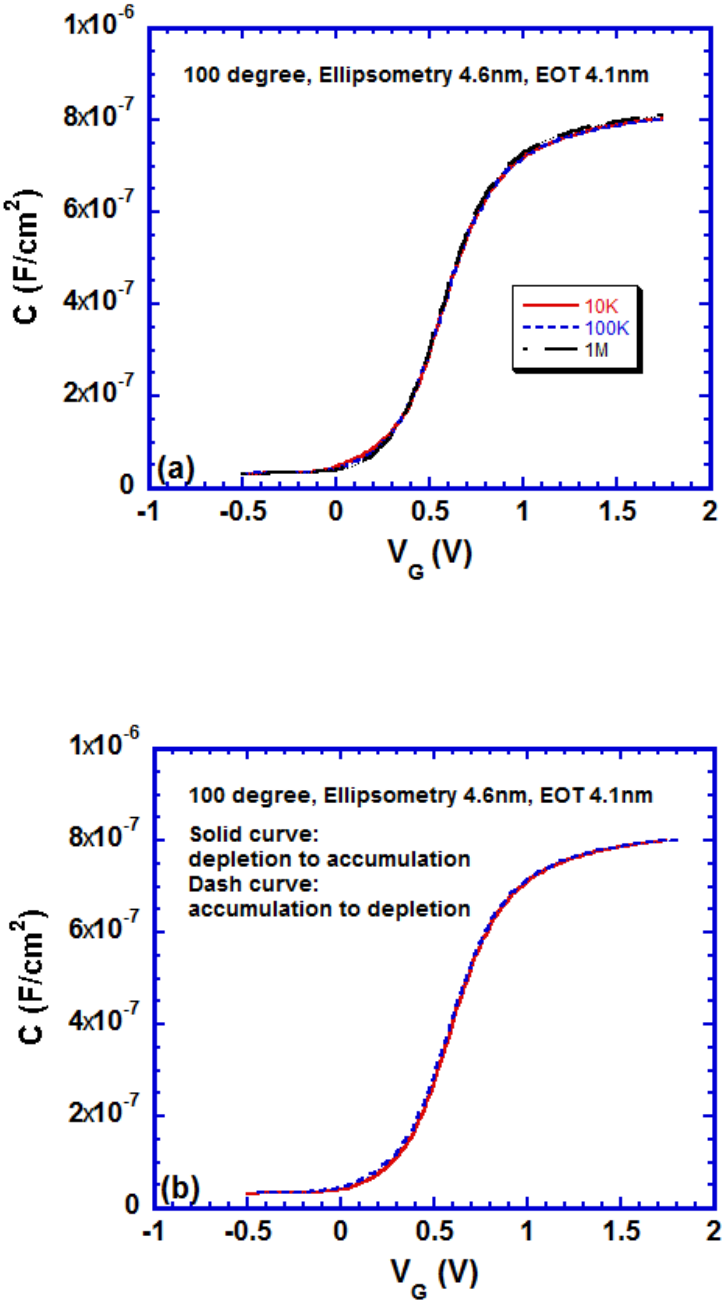


Fig 4.9. (a) Frequency dispersion of C-V curves of MOS capacitor using ALD SiO_2 deposited at 100^0C as gate dielectric. (b) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in figure 9(a).

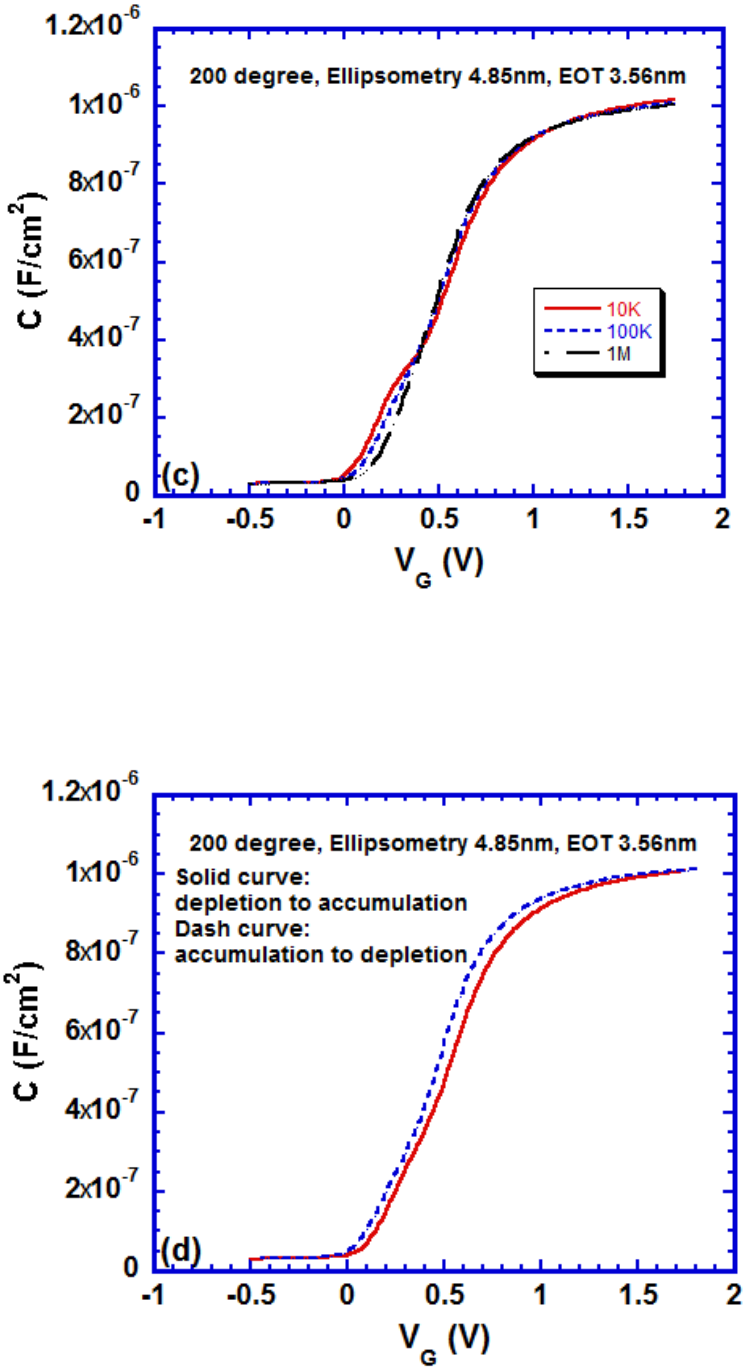


Fig 4.9. (c) Frequency dispersion of C-V curves of MOS capacitor using ALD SiO_2 deposited at 200^0C as gate dielectric. (d) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in figure 9(c).

Chapter 5 Atomic layer deposition of HfO_2 using chemical oxide as an interfacial layer

5.1 Introduction

HfO_2 has become the mainstream high-k dielectric material in semiconductor industry. The application of HfO_2 in complementary metal oxide semiconductor (CMOS) technology is the basis of the continuous scaling of integrated circuits and microprocessor. Among various dielectric materials with high dielectric constant (high-k), HfO_2 became the top selection because of its excellent material and electrical properties such as high dielectric constant (~20), sufficient band offset with Si, large bandgap (5.6-5.8 eV), good thermodynamic stability, etc.[1-7]. It has been proved that HfO_2 is compatible with the self-aligned process in the conventional CMOS technology (>1000°C) [8-12], so it can be easily integrated into the well-established industry process without introducing additional technical barriers.

The success of HfO_2 as an ideal gate dielectric is contributed to the superior quality of HfO_2 films obtained by Atomic Layer Deposition (ALD). ALD provides precise control of film thickness, stoichiometry and uniformity at the atomic scale, due to its self-limiting surface reaction [4, 6, 13]. However, not all surfaces are suitable for ALD deposition. Unlike the flawless interface between Si and thermally grown SiO_2, direct deposition of HfO_2 on Si substrate would introduce interface trap charges and defects, and harm the qualities of MOS devices.

Extensive work has been done to investigate the proper interface conditions for ALD of metal oxides. It is widely accepted that non-oxide like Si surface creates barrier for initial cycles of ALD, results in growth incubation period [14-16]. ALD of high-k materials on –H terminated Si surface exhibits heterogeneous island growth instead of uniform growth, and the gate leakage current of the deposited thin films was reported to be high[14-18]. Researchers such as E. P. Gusev, etc. and R. L. Puurunen, etc. explored the ALD nucleation of ZrO_2, Al_2O_3, TiO_2 and HfO_2 on Si surface, and proved that comparing to nucleation on SiO_2 surface, nucleation on H-terminated Si surface is characterized by non-uniformity, island-like morphology, poor metal oxide qualities, and metal diffusion at high temperature[13, 17, 19-24]. Plus, underlying SiO_2 would grow at the Si/metal oxide interface at moderate temperature, which is harmful to the scaling of MOS devices[25, 26]. The regrowth of the SiO_2 has been proved by infrared spectroscopy[27]. There are also researches on nucleation of HfO_2 on Si (110) and Si (111)[28], and Ge surface[29, 30], which is a potential substrate material with high mobility. L. Nyns, etc. further explored the initial few cycles of the ALD process on H-terminated, OH-terminated Si surface and different Si orientations.

Hydroxyl group (-OH) termination of Si is crucial for the chemical attachment of Hf precursor onto the Si surface. Si surface terminated by –OH groups is hydrophilic. An interfacial layer between Si substrate and HfO_2 dielectric layer is necessary to provide –OH terminated hydrophilic surface for the initial nucleation of ALD. The interfacial layer also helps to decrease the interface trap charges and defects. An ultrathin layer of SiO_2-like interface full of –OH groups and highly hydrophilic is desirable as the initial surface for

ALD of HfO_2. Meanwhile, since the dielectric constant of the interfacial layer is low (~3.9), the physical thickness of the interfacial layer should be minimized, in order not to harm the equivalent oxide thickness (EOT) of the whole gate oxide stack.

5.2 Growth of chemical oxide as an interfacial layer

Green, etc. did extensive work to compare the nucleation and growth of HfO_2 on Si surfaces with various pre-deposition treatments[31]. The Si surfaces are listed as follow: -H terminated Si surface obtained by HF etching; DI water (de-ionized water) and ozone processed Si surface; chemical oxide grown by SC 1 solution (H_2O, H_2O_2 and NH_3OH); chemical oxide grown by SC 2 solution (H_2O, H_2O_2 and HCl); thermal SiO_2 grown by rapid thermal oxidation; and Si-O-N grown by rapid thermal oxynitride. Among these pre-deposition treatments, chemical oxide prepared by SC 1 solution results in minimum ALD nucleation barrier. The deposition of HfO_2 films on this chemical oxide is linear and conformal, with high coverage rate, small film roughness, and film density close to theoretical value. Meanwhile, the chemical oxide prepared by SC 1 solution is very thin (only ~0.5 nm), which is desirable to meet the continuous scaling requirement on the high-k gate dielectric[31]. This pre-treatment of Si surface has been applied by other research groups because of its appealing interfacial quality[1, 18].

The thickness of chemical oxide interface layer is crucial for the scaling of the gate dielectric stack. Also, since HfO_2 films will be deposited onto the interfacial layer, the thickness of the SiO_2-like interfacial layer is necessary for the spectroscopic ellipsometry (SE) measurement of the ALD HfO_2 films. The growth of chemical oxide in SC 1 solution

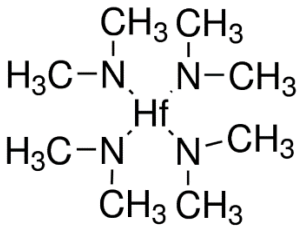
has been studied in details. Boron doped p type Si(100) wafers with a resistivity of 1-20 Ω cm were used as substrates. Before the growth of chemical oxide, the substrates were cleaned using Radio Corporation of America (RCA) cleaning to remove organic and ionic contaminations. H-terminated Si surface was achieved by immersing Si substrates into diluted buffered oxide etch (BOE, 6:1 with surfactant) solution (DI H_2O: BOE=80ml: 20ml). The composition of the SC 1 solution was: 200ml DI H_2O:4ml H_2O_2 (30 wt%):2ml NH_4OH (NH_3; 29 wt%). The chemical oxide was grown at 45°C, 60°C and 80°C. The thicknesses of the chemical oxide layers were measured using SE, and the results are listed in Table 5.1.

As illustrated in Chapter 4, a "baseline" exists when using SE to measure SiO_2 <12Å. The "baseline" value is the thickness that the SE system displays when measuring a fully hydrophobic Si surface without any oxide. The physical thickness of the ultrathin oxide layer should be the SE system displayed value subtracted by the baseline value, which is 8.99Å here. In Chapter 4, the baseline value was 7.49Å. This is because the baseline value was measured every time before the measurement of ultrathin oxide layers, in order to compensate the measuring error of the SE system. In table 5.1, T_{ch} is the ellipsometry reading of the chemical oxide, and T_0 (8.99Å) is the baseline value.

5.3 Atomic layer deposition of HfO_2 using chemical oxide as an interfacial layer

Using chemical oxide as the interfacial layer, HfO_2 films was grown by ALD. The ALD system was produced by *Cambridge Nanotech Inc*. After growth of chemical oxide, Si

substrate was loaded into ALD chamber immediately at 100°C. HfO_2 was deposited using tetrakis(dimethylamino)hafnium (TDMAH) as the metal organic precursor and DI H_2O as the oxidant. The structure of TDMAH is



The temperature of TDMAH was increased to 75°C to provide enough vapor pressure. HfO_2 films was deposited at 300°C. It took about 20 minutes to increase the chamber temperature from 100°C to 300°C in our ALD system. We loaded the substrate at 100°C in order to avoid regrowth of the Si substrate, as well as the stress accumulation in the HfO_2 thin films due to the sudden change of temperature. The carrier gas was nitrogen at a flow rate of 20 sccm (standard cubic centimeters per minute). TDMAH and DI H_2O were supplied into the chamber sequentially with TDMAH comes first. The pulse times were chosen to meet the saturation requirement of ALD. The details of the deposition parameters are summarized in table 5.2. Increasing the pump time from 5 seconds to 20 seconds would slightly improve the uniformity of the deposited films, but the improvement is subtle and does not worth the additional time consumption.

Figure 5.1 shows the growth linearity of ALD HfO_2 using chemical oxide as an interfacial layer. HfO_2 was deposited for 35, 50, 75 and 100 cycles. The physical thicknesses of HfO_2 films were measured by SE using chemical oxide as a built-in initial layer. The growth of HfO_2 shows excellent linearity without incubation period, suggesting good nucleation even

in the beginning cycles and a stable atomic-layer-by-atomic-layer deposition. The deposition rate of 0.9-1Å/cycle was extracted by calculating the slope of the straight growth line.

5.4 The dependence of interfacial quality on the thickness of the chemical oxide interfacial layer

MOS capacitors were fabricated and tested to explore the dependence of interfacial quality on the thickness of the chemical oxide interfacial layer. Titanium (Ti, 100Å) and nickel (Ni, 1000Å) were deposited by electron-beam evaporation as gate metals. Ti is added here to enhance adhesion between the gate metal and the dielectric stack. The metal gates were patterned by photolithography and wet etching. The gate patterns were circles and the diameter was 100μm. The details of the wet etching process are described in Chapter 2. The backside of the Si substrates was coated by aluminum (1000Å). The samples were then annealed at 450°C in forming gas (N_2:H_2=10:1) for 30 minutes to create Ohmic contact between Al and bulk Si. The Capacitance density-Voltage (C-V) curves of the MOS capacitors were measured using an Agilent 4284A LCR meter at 100 KHz, and the Current density-Voltage (J-V) curves were measured using an Agilent 4155B semiconductor parameter analyzer. Equivalent oxide thickness (EOT) and flatband voltage (V_{FB}) were extracted by fitting the 100 KHz C-V curves with the theoretical quasi-static C-V simulation (UC Berkeley's quantum-mechanical C-V simulator).

Theoretical simulation suggested that the minimum thickness of the chemical oxide layer is ~ 0.4 nm in order to maintain a high quality interface[32]. We did explicit experiments

to prove this theoretical simulation. Chemical oxide interfacial layers were grown in SC 1 solution at 60°C for 1 minute, 2 minutes and 4 minutes, and the resulting physical thicknesses of the interfacial layers were 0.4 nm, 0.45 nm and 0.5 nm, respectively. 35 cycles of ALD HfO_2 was deposited on these three interfacial layers. The C-V curves of the MOS capacitors using the chemical oxide/35-cycles-ALD HfO_2 as gate dielectric are displayed in figure 5.2 (a)-(c). The dots are the experimental data, and the solid curves are the theoretical quasi-static C-V simulation. In figure 5.2(a), the chemical oxide was grown in SC 1 solution for 1 minute and the physical thickness is 0.4 nm. The C-V curve does not increase sharply from depletion region to accumulation region, and it deviates from the theoretical simulation curve, which suggests high density of interface traps. We increased the thickness of HfO_2 film by running ALD deposition for 50 cycles, and the C-V curve of the corresponding MOS capacitors is also displayed in figure 5.2(a) by the solid squares. This C-V curve also shows deviation from the theoretical simulation curve. The deviation is alleviated comparing to the C-V curve of the MOS capacitors using 35 cycles ALD HfO_2, but it is still obvious. The 0.4 nm chemical oxide is too thin and could not be used as an ALD interfacial layer with good quality.

Figure 5.2(b) shows the C-V curve of the MOS capacitors using 0.45 nm chemical oxide as the interfacial layer. The C-V curve is notably improved: it increases sharply from depletion region to accumulation region, and the fitting with the theoretical C-V simulation is good. The good fitting suggests the interface trap density is small. The 0.45 nm chemical oxide could be used as a reliable interfacial layer for ALD of HfO_2. The C-V curve of the MOS capacitors using 0.5 nm chemical oxide as the interfacial layer is displayed in figure

5.2(c). Comparing figure 5.2(c) to figure 5.2(b), the fitting between the experimental data and the theoretical C-V simulation is not further improved. Considering the continuous scaling requirement on the MOS gate dielectric stack, the 0.45 nm chemical oxide is more preferable as an interfacial layer.

J-V curve of the MOS capacitors using 0.45 nm chemical oxide/35-cycles-ALD HfO_2 as gate dielectric is shown in figure 5.3. The gate leakage current density matches other reported data [20, 33, 34].

5.5 Conclusion

4.5 Å is the minimum thickness needed for the chemical oxide to be a high quality interface for ALD of HfO_2 on Si. Growing chemical oxide in SC 1 solution at 60°C for 2 minutes is a reliable method to provide desirable interfacial layer. This method would be applied in the following works as a reference to evaluate the qualities of innovative interfacial layers.

Table 5.1. Spectroscopic Ellipsometry (SE) measured thickness of the chemical oxide layers grown using the SC 1 solution with different parameters (oxidation temperature and time). T_0 (8.99Å) is the baseline value; T_{ch} is the ellipsometry reading of the chemical oxide.

Time (min)		**1**	**2**	**5**	**7**
45°C	**T_{ch} (Å)**	12.84	13.37	———	13.72
	($T_{ch} - T_0$) (Å)	**3.85**	**4.38**	———	**4.73**
60°C	**T_{ch} (Å)**	12.81	13.50	14.54	———
	($T_{ch} - T_0$) (Å)	**3.82**	**4.51**	**5.55**	———
80°C	**T_{ch} (Å)**	13.02	13.93	———	———
	($T_{ch} - T_0$) (Å)	**4.03**	**4.94**	———	———

Table 5.2: ALD program for deposition of HfO_2 using TDMAH and DI H_2O at 300^0C.

Susceptor temperature = 300°C, wall temperature = 250°C			
Precursor	Pulse time (sec)	Exposure time(sec)	Pump time (sec)
TDMAH	0.5	0	5
DI H2O	0.5	0	5

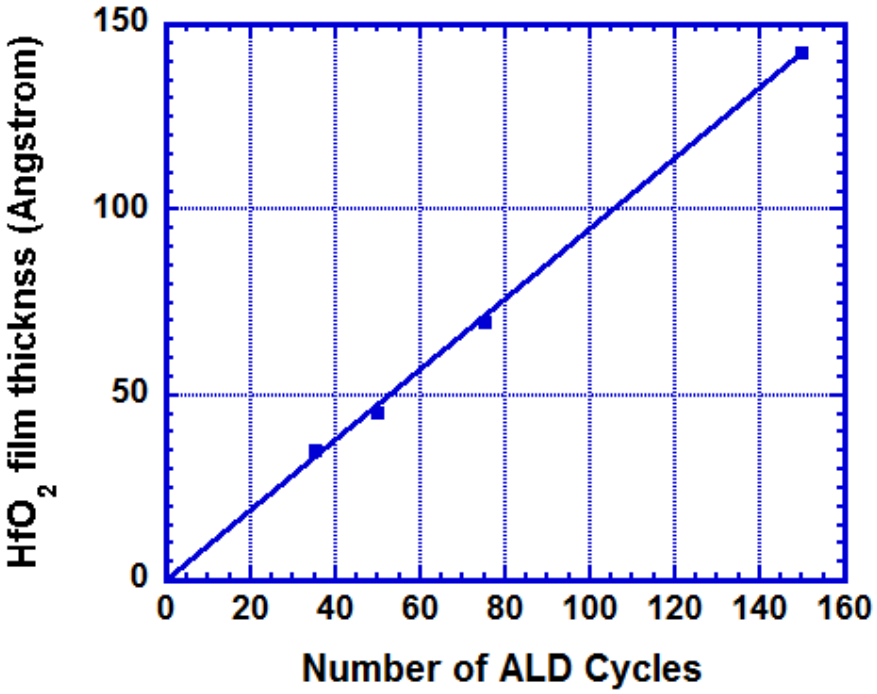


Figure 5.1. Growth linearity of ALD HfO_2 using chemical oxide as an interfacial layer. HfO_2 was deposited for 35, 50, 75 and 150 cycles.

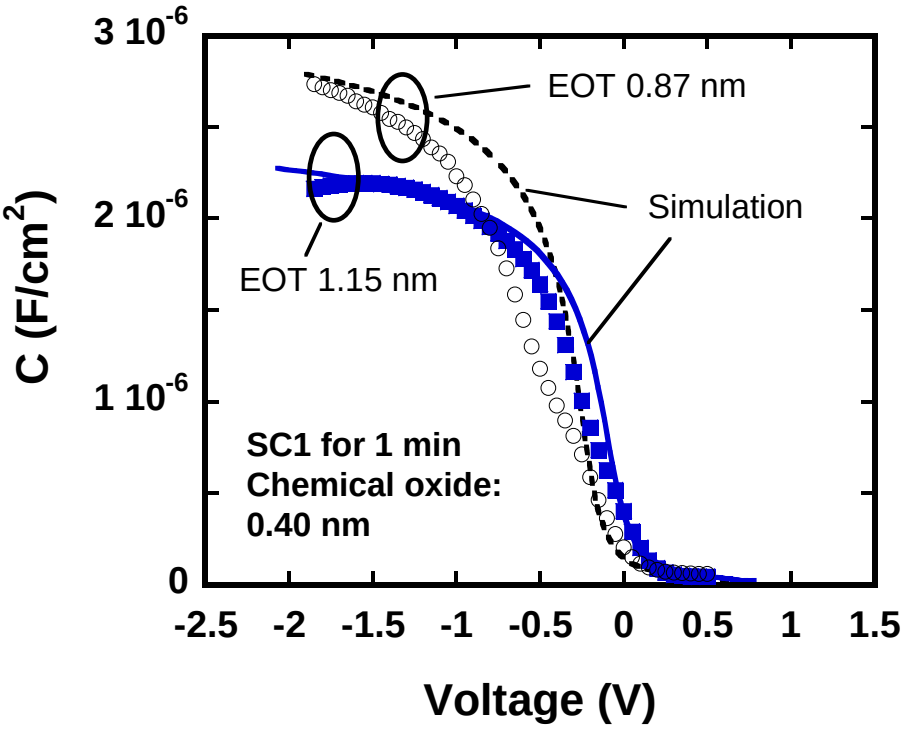


Figure 5.2. (a) Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curves were measured at 100 KHz. The interfacial layer was grown in SC1 solution at 60°C for 1 minute, and the thickness is 0.40 nm. The HfO_2 films were deposited for 35 cycles (circles) and 50 cycles (squares).

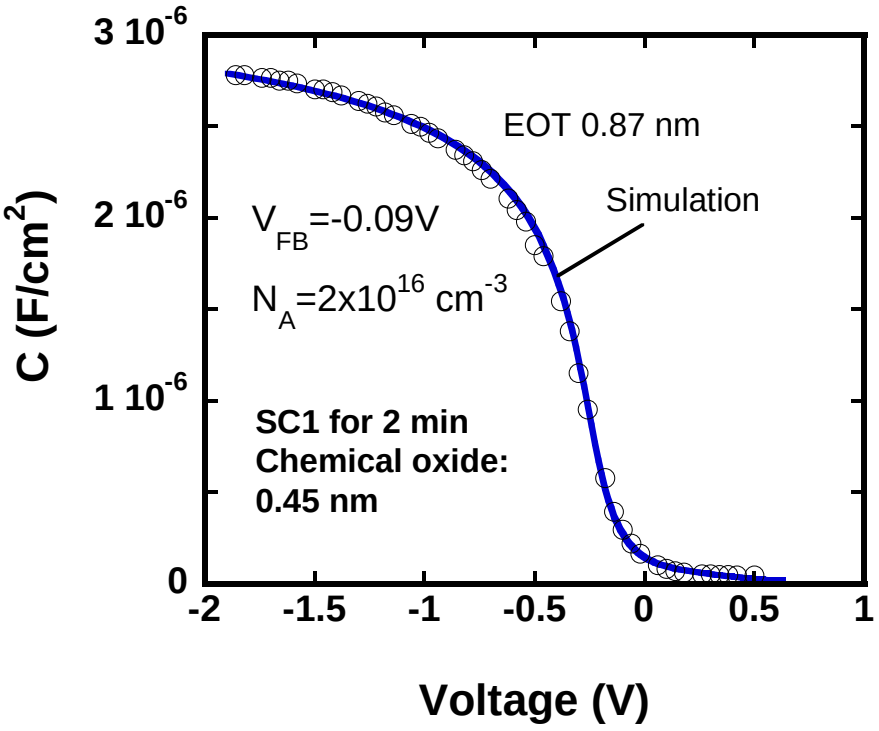


Figure 5.2. (b) Experimental (dots) and simulated (line) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curve was measured at 100 KHz. The interfacial layer was grown in SC1 solution at 60°C for 2 minutes, and the thickness is 0.45 nm. The HfO_2 film was deposited for 35 cycles.

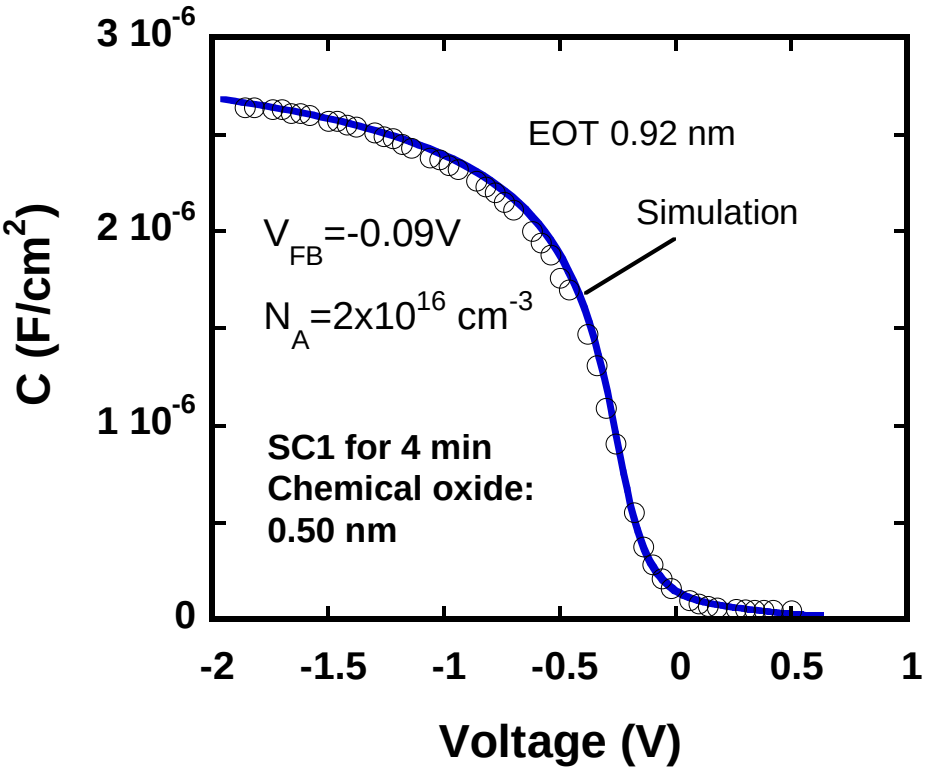


Figure 5.2. (c) Experimental (dots) and simulated (line) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curve was measured at 100 KHz. The interfacial layer was grown in SC1 solution at 60°C for 4 minutes, and the thickness is 0.50 nm. The HfO_2 film was deposited for 35 cycles.

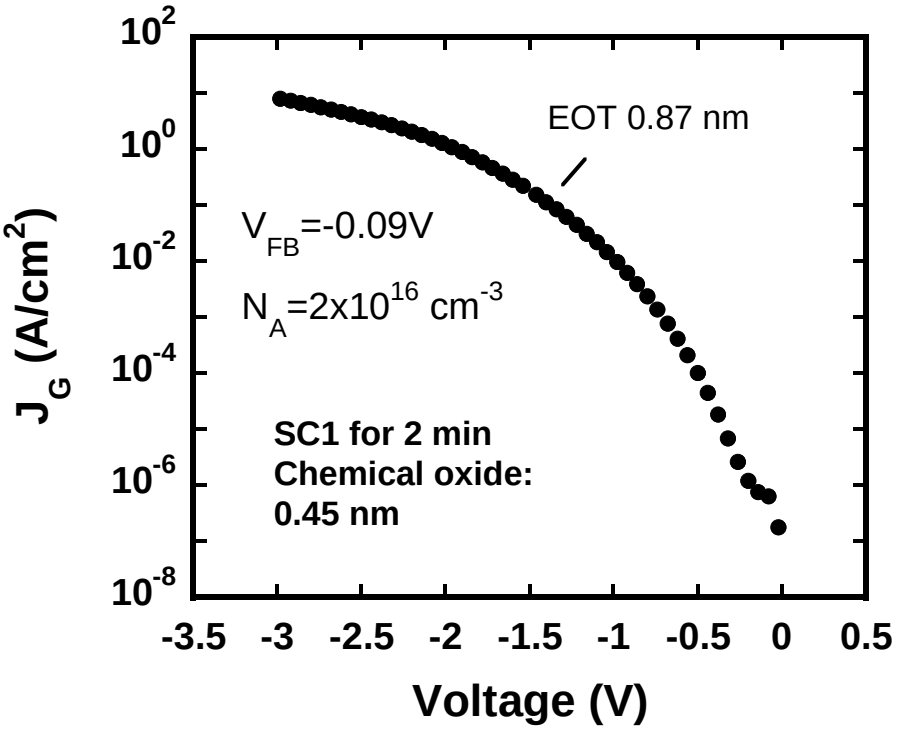


Figure 5.3. J-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The interfacial layer was grown in SC1 solution at 60°C for 2 minutes, and the thickness is 0.45 nm. The HfO_2 film was deposited for 35 cycles.

Chapter 6 Atomic layer deposition of HfO_2 using in-situ formed hydrophilic oxide as an interfacial layer

6.1 Introduction

High-quality HfO_2 can only be grown using ALD on hydrophilic surface, i.e. OH terminated surface. OH termination of Si is crucial for the chemical attachment of metal precursors onto Si surface[1-6]. It was found that the density of –OH groups on Si surface has an effect on the atomic surface roughness and dielectric leakage current of HfO_2[7]. Green et al. demonstrated that chemical oxide grown by SC1 solution ($1NH_4OH:4H_2O_2:200H_2O$) is full of –OH groups and works effectively as an interfacial layer for ALD growth of HfO_2[8]. This was proved in our group, and the experiment details are discussed in Chapter 5. Ozone based wet chemical oxidation and ozonated water spraying are widely used in industry for ALD growth of HfO_2 [9, 10]. The growth of the interfacial layer was controlled by ozone concentration in water. However, in 3-D silicon MOS devices structures, such as FinFETs and nanowire FETs, it is difficult to allow uniform oxide formation on the sides of the fins and underneath the nanowire in wet chemical solution or by spraying.

In this work, we report an ALD-based in-situ formation of SiO_2 interfacial layer using one cycle of ozone and water. The interfacial layer formed is highly hydrophilic, and the ALD HfO_2 grown on this interfacial layer has comparable qualities to HfO_2 grown on SC1 chemical oxide. The interfacial layer was in-situ formed in the ALD chamber. This method might be used in sophisticated 3-D MOS structures because ALD allows molecules to be deposited on the surface that cannot be accessible using other methods. In addition, the

chemical oxidation step can be eliminated from the integrated circuits manufacturing processes, which is economically beneficial to the industry.

6.2 Experimental

Boron doped p type Si(100) wafers with a resistivity of 1-20 Ω cm were used as substrates. The substrates were cleaned using Radio Corporation of America (RCA) cleaning to remove organic and ionic contaminations. H-terminated Si surface was achieved by immersing Si substrates into BOE (buffered oxide etch) solution. After BOE etching, Si substrate was loaded into ALD chamber (*Cambridge Nanotech Inc*) immediately at 100°C. Then the surface was exposed to 1 ALD cycle of ozone (O_3) and deionized water (DI H_2O), which were introduced into ALD chamber sequentially with ozone coming first. O_3 was produced from O_2 by an ozone generator (*A2Z Ozone Inc*.). It was found that after this process, an ultrathin layer of SiO_2 was thermally grown on Si substrate, and the surface of the SiO_2 is highly hydrophilic. Usually Si could not be effectively oxidized by O_2 at temperature below 500°C; O_3 is a strong oxidant, and can grow desired ultrathin oxide layer with only one pulse. The H_2O pulse was supplied to provide –OH groups on the interfacial layer surface. The details of this process are listed as following: O_3 pulse time is 0.3 second, exposure time is 30 seconds, pump time is 23 seconds; H_2O pulse time is 0.5 second, exposure time is 15 seconds, pump time is 20 seconds. The pulse and exposure times of ozone and DI water were carefully chosen to minimize the thickness of the SiO_2 layer, so that the equivalent oxide thickness (EOT) of the gate dielectric stack is minimal. Without taking the sample out of the chamber, HfO_2 was deposited on this interfacial layer using tetrakis(dimethylamino)hafnium (TDMAH) and DI water at 300°C, and the pulse

times were chosen to meet the saturation requirement of ALD (TDMAH and H_2O pulse time: 0.5 second. Exposure time: 0 second. Pump time: 5 seconds). Details of the HfO_2 deposition by ALD were described in Chapter 5. As a control sample, chemical oxide was also grown using SC 1 solution ($NH_4OH:H_2O_2:H_2O$=2:4:200) at 60°C for 2 minutes, and HfO_2 was deposited using the same parameters as the ones used on the in-situ formed interfacial layer. This component ratio of SC 1 solution was developed by M. L. Green, etc.[8], and was modified in our previous work to be an effective method to grow interfacial layer for ALD of high quality HfO_2[11] (see Chapter 5 for details). Multi-angle spectroscopic ellipsometry (*J. A. Woollam* M3000V) was used to measure the physical thickness and characterize the optical properties of the thin films.

MOS capacitors were fabricated to electrically evaluate the effectiveness of the interfacial layer/HfO_2 stacks as gate dielectric materials. Titanium (Ti, 100Å) and nickel (Ni, 1000Å) were deposited by electron-beam evaporation as gate metals, because Ti enhances adhesion between the gate metal and the dielectric stacks. The metal gates were patterned by photolithography and wet etching. The gate patterns were circles and the diameter was 100μm. The backside of the Si substrates was coated by aluminum (1000Å). The samples were then annealed at 450°C in forming gas ($N_2:H_2$=10:1) for 30 minutes to create Ohmic contact between Al and bulk Si. The capacitance-voltage (C-V) curves of the MOS capacitors were measured using an Agilent 4284A LCR meter at multi-frequencies, and the current-voltage (I-V) curves were measured using an Agilent 4155B semiconductor parameter analyzer. Equivalent oxide thickness (EOT) and flatband voltage (V_{FB}) were

extracted by fitting the 100 KHz C-V curves with the theoretical quasi-static C-V simulation (UC Berkeley's quantum-mechanical C-V simulator).

6.3 Results and Discussion

6.3.1 Characterization of the in-situ formed interfacial layer

The growth of chemical oxide in SC1 solution has been extensively investigated in our lab before[11]. The physical thickness of the ultrathin chemical oxide grown at the condition described above was ~4.5Å. The chemical oxide thin film was full of –OH groups and highly hydrophilic on the surface. Our in-situ formed SiO_2-based interfacial layer grown by 1 ALD cycle of O_3 and H_2O had similar hydrophilic surface as chemical oxide based on observation. The physical thickness of the in-situ formed interfacial layer was ~3.5Å measured by spectroscopic ellipsometry, which is ~1Å thinner than that of the chemical oxide. This is beneficial to further scaling of the gate dielectric stack. Usually H-terminated Si surface would only be oxidized at elevated temperature (>600°C), not at the temperature (100°C) for our in-situ interfacial layer formation process. The H-termination of Si surface could remain for about 10 minutes in air at room temperature. The successful growth of our in-situ interfacial layer is because O_3 is a stronger oxidant than O_2, and the oxygen atoms dissociated from O_3 molecules directly attack the back bonds of Si[12]. The thin oxide film grown by O_3 was also reported with a stable Si-O-Si network even formed at low temperature[12]. Comparable mean squared errors (MSEs) of the spectroscopic ellipsometry measurements were observed between the chemical oxide and the in-situ interfacial layer (both <5), indicating that the material structures of these SiO_2-based interfacial layers are close to that of the theoretically calculated ideal SiO_2. Therefore, the

oxide quality of our newly developed in-situ interfacial layer is not degraded comparing to that of the chemical oxide.

The interfacial layers prepared by different methods before depositing HfO_2 were characterized by the Thermo Scientific™ K-Alpha™ X-ray Photoelectron Spectrometer (XPS) using an Aluminum Kα micro-focused monochromatic X-ray source with a 400 μm spot size. The depth profile was obtained by an Ar Ion gun of 1000 eV energy with 5 seconds for each layer (the estimated etching speed is 0.5 nm/s for Ta_2O_5).

Figure 6.1 is the main atomic percentage change of main components (Si and O) of chemical oxide interface and O_3+H_2O interface from XPS depth profiling (layer1: the bare surface, layer3: the most in-depth layer). In layer 1, the Si and O atomic percentages of the two interfacial layers are similar to each other. The ratio of Si: O is far away from the ideal 1:2 of SiO_2 and the Si amount is much higher. This phenomenon could be attributed to following reasons: (1) the interfacial layers are ultrathin (<5Å), X-ray could easily penetrate through, and the signal would be affected by the Si substrate. (2) Si substrate cannot be fully oxidized by either the chemical oxidation method or the O_3+H_2O method. (3) Estimation of atomic percentage by XPS is a rough method, the results could be significantly affected by contamination and equipment limitation. From layer 1 to layer 3, the Si:O ratio increases faster in O_3 and H_2O formed interfacial layer, which is because the O_3 and H_2O formed interfacial layer is thinner than the chemical oxide, so the X-ray arrives the Si substrate sooner.

Figure 6.2 displays the oxygen 1s spectrum of the surface of interfacial layers from different treatments before depositing HfO_2. Figure 6.2(a) is from chemical oxide interface, figure 6.2(b) is from O_3+H_2O interface, and figure 6.2(c) is from the surface of Si after only one pulse of O_3. Our O-1s spectrum show that the main chemical states of oxygen on the surface are hydroxyl (~ 531.5 eV)[13], Si-O(~ 532.5 eV)[13] and H_2O (~534 eV)[14], but their amounts (the area under each peak) on the surfaces vary between different preparation methods.

Comparing chemical oxide (Figure 6.2a) and O_3+H_2O (Figure 6.2b) methods, the amount of –OH group on the surface interface from O_3+H_2O method (area under –OH peak : area under Si-O peak is 0.24) is smaller than that on the interface from chemical oxide method (area under –OH peak : area under Si-O peak is 0.57). Introducing H_2O in the end of O_3 process is necessary, since the amount of –OH group on the interface from O_3+H_2O process is increased comparing with O_3 only method (area under –OH peak : area under Si-O peak is 0.17).

6.3.2 Growth linearity of ALD HfO_2 on in-situ formed interfacial layer

After formation of the interface layer, the substrate temperature was increased to 300°C. During the temperature ramping up, the samples remained in the ALD vacuum chamber, so there was no unwanted SiO_2 re-growth. Therefore, it is an in-situ deposition process. At 300°C, HfO_2 was deposited on the samples by ALD for 15, 21, 24, 35, 50, 100, 150 and 200 cycles. The physical thicknesses were measured using spectroscopic ellipsometry as shown in Figure 6.3(a) with square marks. The MSE of the measurement is less than 5.

The growth of HfO_2 shows excellent linearity even during the starting cycls, suggesting a stable atomic-layer-by-atomic-layer deposition. The deposition rate of ~1Å/cycle was extracted by calculating the slope of the straight growth line. MOS capacitors were fabricated using the interfacial layer/HfO_2 stacks as the gate dielectric. The EOTs of the gate dielectric stacks were extracted from the C-V curves measured at high frequency (100 KHz), which were plotted in Figure 6.3(a) with triangle marks. Several devices were measured for each number of ALD cycles, and the EOTs have variation <2Å among all the measured devices. The linearity of EOT vs. ALD cycle numbers will be discussed in details later.

Figure 6.3(b) shows the physical thickness of HfO_2 deposited for 1, 2, 3, 4, 5, 10 and 30 cycles on chemical oxide interface and O_3+H_2O interface. During 1-5 cycles, the growth of HfO_2 is not linear. The HfO_2 growth tracks on these two interfacial layers are similar, which implies the O_3+H_2O interface is as effective as the chemical oxide interface. The MSEs of the spectroscopic ellipsometry measurements are 3-4, and the error bar would mix together with the data point mark, so it is not shown in figure 6.3(b).

6.3.3 Electrical characterization of MOS capacitors

Figures 6.4 and 6.5 are the high frequency (100 KHz) Capacitance density-Voltage (C-V) curves of the MOS capacitors using the in-situ formed interfacial layer/ALD HfO_2 as the gate dielectric stacks. HfO_2 was deposited for 21 cycles on the sample shown in Figure 6.4, and 24 cycles on the sample shown in Figure 5. In Figure 6.4, the C-V curve of the MOS capacitor using ALD HfO_2 deposited for 21 cycles on the chemical oxide is also plotted as

a reference. The dots are the measurement data (circles are data from the chemical oxide sample and squares are data from the in-situ formed interfacial layer sample), and the solid curves are the theoretical quasi-static C-V simulation that takes quantum effects into consideration. In all the C-V results, the deviation of capacitance density is under 5×10^{-8} F/cm^2. This is too small to be drawn as an error bar, since the error bar would mix together with the data point. The fitting of the simulation to the measurement data is precise in the depletion region and in the initial part of the accumulation region. In the high-voltage part of the accumulation region, the measurement data have deformation and the capacitance value drops. This is because the interfacial layer plus the 21-cycle-ALD HfO_2 stack is ultrathin with its physical thickness of < 3 nm, so that the direct tunneling current through the dielectric stack is high, which causes C-V deformation in the high gate voltage region[15]. By fitting the measurement data with simulation, we extracted the flatband voltage (V_{FB}) and the EOT of the capacitors. The physical thicknesses of the HfO_2 thin films are also marked in the Figures. The physical thicknesses of the HfO_2 films on these two samples are 2.59 nm and 2.79 nm, separately, and the corresponding EOTs are 0.86 nm and 0.98 nm. The HfO_2 physical thickness of the in-situ formed interfacial layer sample is 2Å thinner than that of the chemical oxide sample, which was caused by experiment variation. The 2Å difference in physical thickness corresponds to 0.4Å difference in EOT, but the EOT of the in-situ interfacial layer sample is 1.2Å thinner than that of the chemical oxide sample. This extra 0.8Å less EOT should be attributed to the thinner interfacial layer comparing to chemical oxide.

The C-V curve of the MOS capacitors using the in-situ formed interfacial layer plus the 24- cycle-ALD HfO_2 gate stack is plotted in Figure 6.5. The physical thickness of HfO_2 on this sample is almost the same as that of the chemical oxide sample, and the EOT is slightly thinner (0.4Å) than that of the chemical oxide sample. The thickness of interfacial layers is slightly less than 5Å. The EOTs of the samples in both Figures 6.4 and 6.5 suggest that the quality of HfO_2 deposited on the in-situ formed interfacial layer is comparable to that deposited on the chemical oxide.

MOS capacitors were fabricated using samples with 35, 50 and 100 ALD cycles of HfO_2. The samples were analyzed in the same way as described above, and the EOT vs. cycle number is plotted in Figure 6.3 with the triangle mark. The C-V curves of the capacitors using HfO_2 with cycle numbers of < 21 have large deformation in the accumulation region due to large leakage current. The linearity of EOT vs. ALD cycle numbers is excellent, suggesting that it is a true ALD process.

Figure 6.6 shows the Current density-Voltage (J-V) curves of the capacitors discussed above. The J-V curve of the chemical oxide sample is also plotted as a reference. In all the J-V results, the deviation of the current density is within half order. The uniformity is pretty good among all the measured devices. The gate leakage current is evaluated at $V_G=V_{FB}+1V$. At this gate voltage, the leakage current of the chemical oxide sample is 2.65×10^{-2} A/cm^2, which matches with the previously reported results[16, 17]. The leakage current of the in-situ interfacial layer sample with 21-cycle-ALD HfO_2 is 0.2 A/cm^2, which is 1-order-of-magnitude higher than that of the chemical oxide sample. This is because the EOT of the

in-situ interfacial layer sample is 1.2Å thinner than that of the chemical oxide sample. The physical thickness and EOT of the 24 cycles ALD HfO_2 sample are almost the same as those of the chemical oxide sample, and its gate leakage current is 5.32×10^{-2} A/cm^2, which is also comparable to that of the chemical oxide sample. The gate leakage current of HfO_2 grown by ALD could be affected by the interfacial layer because the initial nucleation is dependent on the interfacial layer. If the interfacial layer is lack of –OH groups, or is not hydrophilic, there are not enough sites on the sample surface for molecules of TDMAH to attach to, so that nucleation is disturbed. In this case, the molecules might be stacked on each other randomly, resulting in HfO_2 films with non-stoichiometry and defects. The gate leakage current of the dielectric stacks using the in-situ formed interfacial layers comparable to that using chemical oxide interfacial layer suggests that this method is useful.

6.3.4 Frequency dispersion and hysteresis of MOS capacitors

In order to further understand the trap charges in the interface and in the HfO_2 thin film, we carried out measurement of frequency dispersion and hysteresis behaviors of the C-V curves, the results are shown in Figure 6.7. The chemical oxide/21-cycles-ALD HfO_2 sample was used as a reference, and the in-situ interfacial layer/24-cycle-ALD HfO_2 sample was studied, because the two samples have the same EOT. Figure 6.7(a) shows three C-V curves of MOS capacitor on the chemical oxide sample, measured at 10 KHz, 100 KHz and 1 MHz, separately. The three curves overlap with each other in depletion region with the same V_{FB}. The C-V curve in accumulation region at 1 MHz does not match with the curves at 10 KHz and 100 KHz. This phenomenon is not caused by interfacial traps, but by the series resistance of the gate electrode [18-20]. The samples were kept in

air for months before we measured the C-V frequency dispersion, and a thin layer of Ni_xO_y would have already formed on the Ni gate surface, which increases the gate series resistance. The C-V curves at 10 KHz and 100 KHz overlapping with each other suggests that there is no frequency dispersion and the interfacial quality is very good. Figure 6.7(b) shows the C-V hysteresis behavior of the same capacitor at 100 KHz. The solid curve in the figure was measured from depletion to accumulation, and the dash curve was measured from accumulation to depletion. The two curves overlap with each other and the V_{FB} shift is negligible, suggesting the mobile charge in the HfO_2 thin film is small. Figures 6.7(c) and 6.7(d) are the C-V frequency dispersion and hysteresis behavior of the in-situ interfacial layer/ALD HfO_2 sample. Figures 6.7(c) and 6.7(d) show C-V curves similar to those in Figures 6.7(a) and 6.7(b): the C-V curves measured at different frequencies are all smooth; the C-V curves measured at different frequencies have the same V_{FB}; the hysteresis behavior is negligible. Therefore, we conclude that the ALD in-situ formed interfacial layer provides comparable interfacial quality and dielectric stack quality to that of the chemical oxide interface.

6.4 Conclusion

In summary, a highly hydrophilic SiO_2-based interfacial layer was in-situ formed in the ALD chamber using 1 cycle of O_3 and DI H_2O. HfO_2 was deposited on this interfacial layer using a conventional ALD process. Studies of interfacial layer characterization, HfO_2 growth linearity, EOT of the stack, gate leakage current, and frequency dispersion and hysteresis behavior of the C-V curves suggest that the in-situ formed interfacial layer can result in the same high-quality HfO_2 dielectric layers as the chemical oxide interfacial layer.

Using this approach, the wet chemical oxidation step can be eliminated from the processes of deposition of high-k gate stacks.

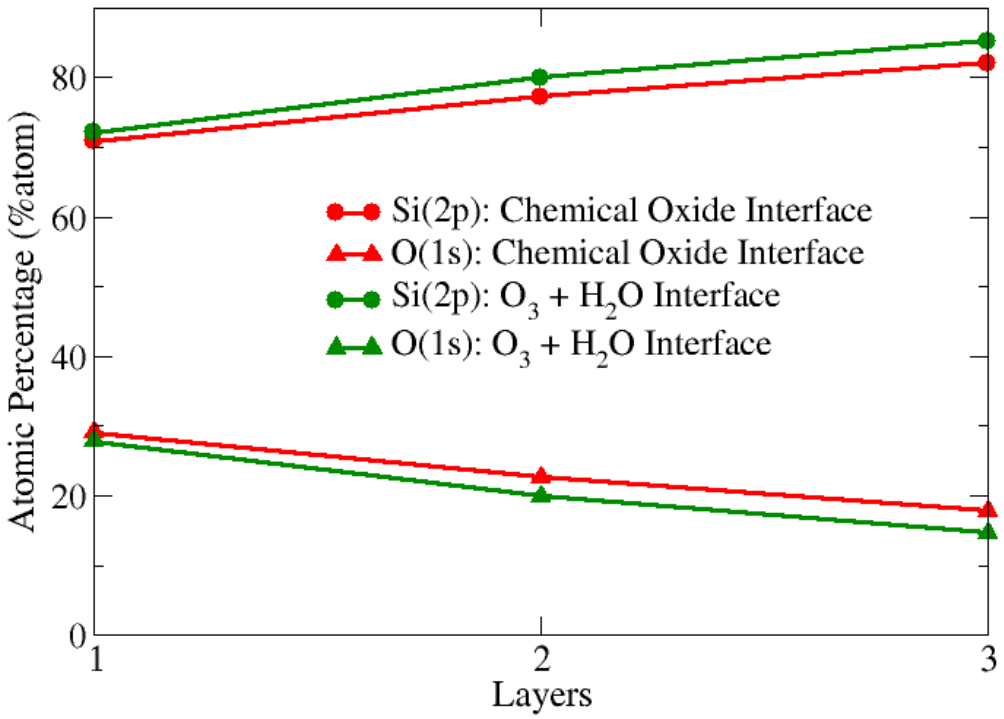


Figure 6.1. The main atomic percentage change of main components (Si and O) of chemical oxide interface and O_3+H_2O interface from XPS depth profiling (layer1: the bare surface, layer3: the most in-depth layer).

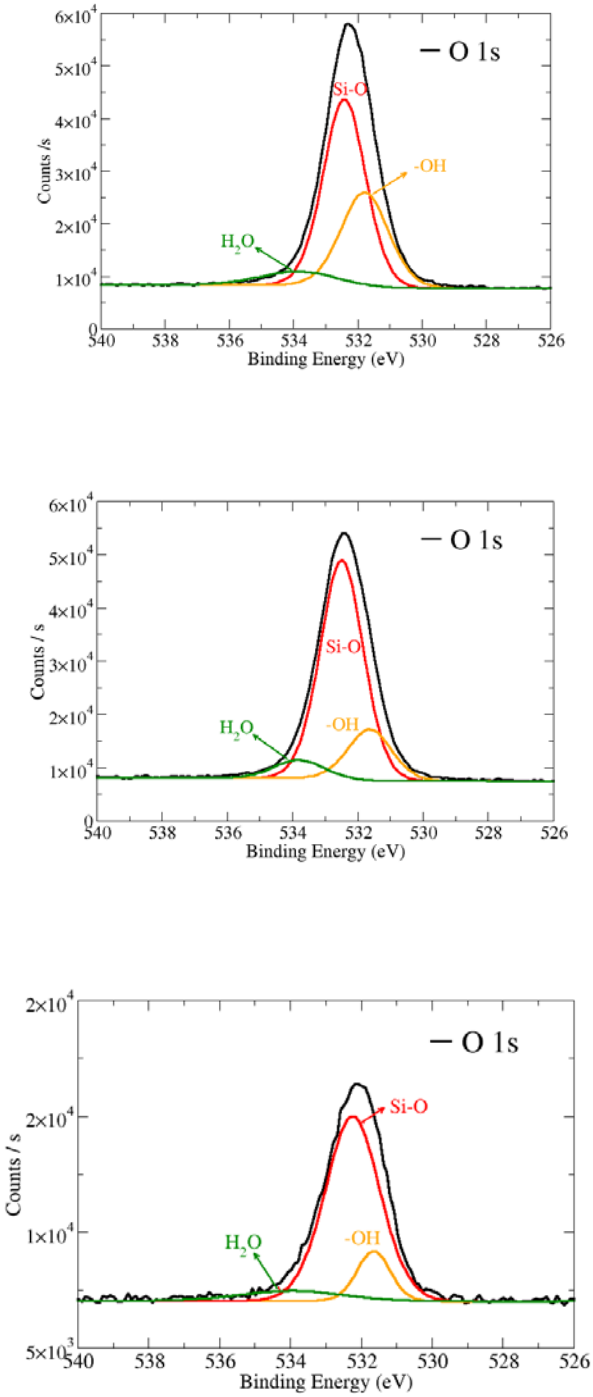


Figure 6.2. (a)-(c): The oxygen 1s spectra of the interfacial layers from different treatments before depositing HfO_2. (a) Chemical oxide interface. (b) O_3+H_2O interface. (c) only O_3 grew interface.

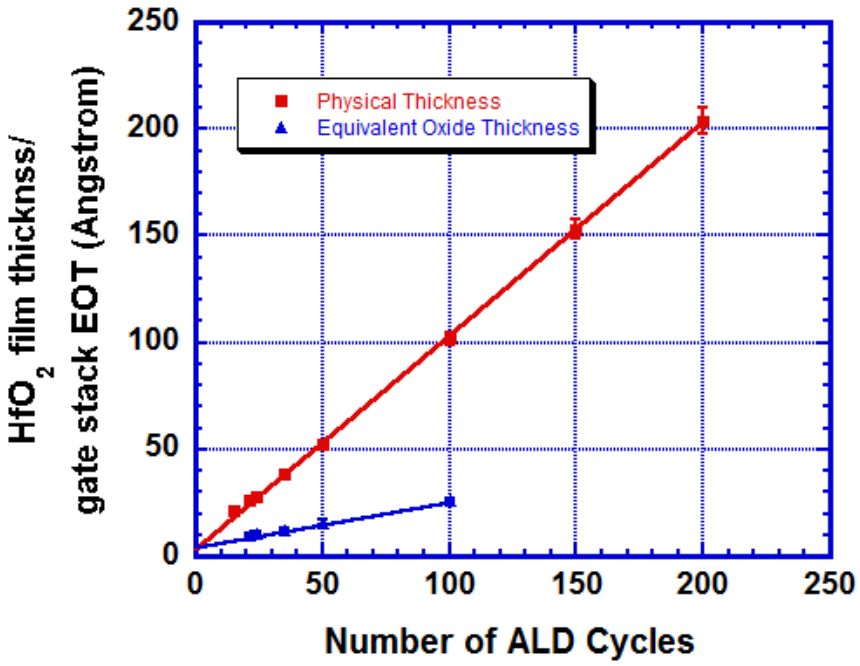


Figure 6.3. (a) Square: Physical thickness of ALD HfO_2 thin films deposited for 15, 21, 24, 35, 50, 100, 150, 200 cycles. Triangle: Equivalent Oxide Thickness (EOT) extracted from high-frequency (100 KHz) capacitance-voltage (C-V) curves of the MOS capacitors using the interfacial layer/HfO_2 as the gate stacks. The interfacial layer was grown by 1 ALD cycle of O_3 and DI H_2O at 100°C. Physical thicknesses of the HfO_2 thin films were obtained by spectroscopic ellipsometry.

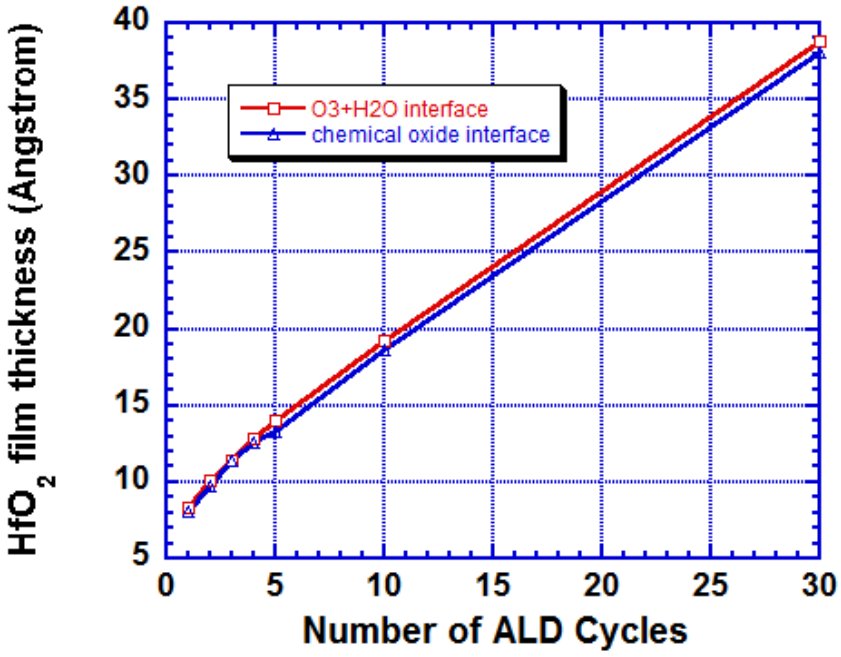


Figure 6.3. (b) ALD of HfO_2 on chemical oxide interface and O_3+H_2O interface for 1, 2, 3, 4, 5, 10, and 30 cycles.

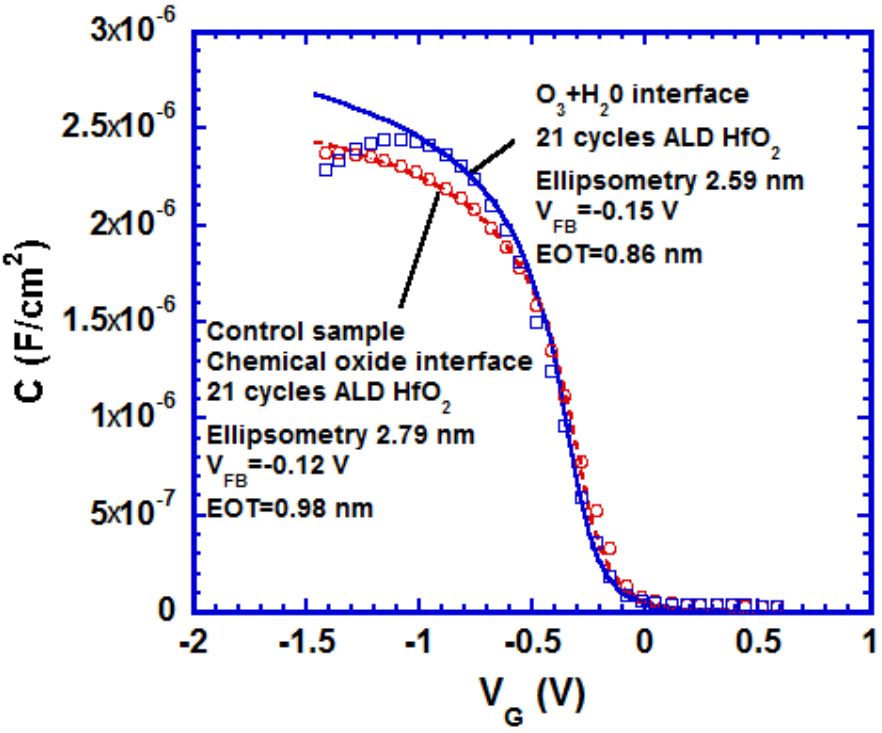


Figure 6.4. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curves were measured at 100 KHz. The interfacial layers were grown by SC1 chemical oxidation and 1 ALD cycle of O_3 and DI H_2O at 100°C, separately. The HfO_2 films were deposited for 21 cycles.

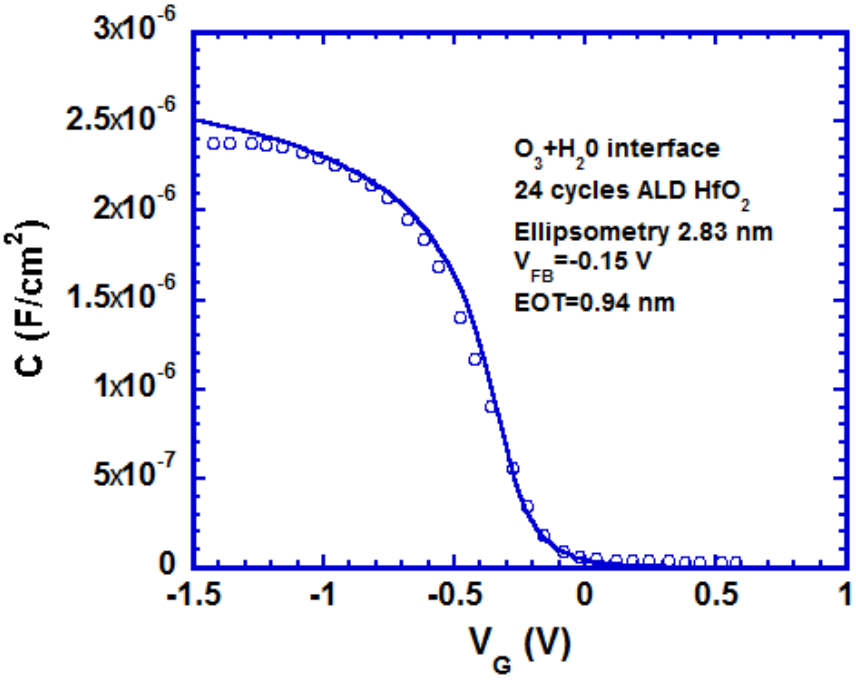


Figure 6.5. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The interfacial layers were grown by 1 ALD cycle of O_3 and H_2O at 100°C. The HfO_2 were deposited for 24 cycles.

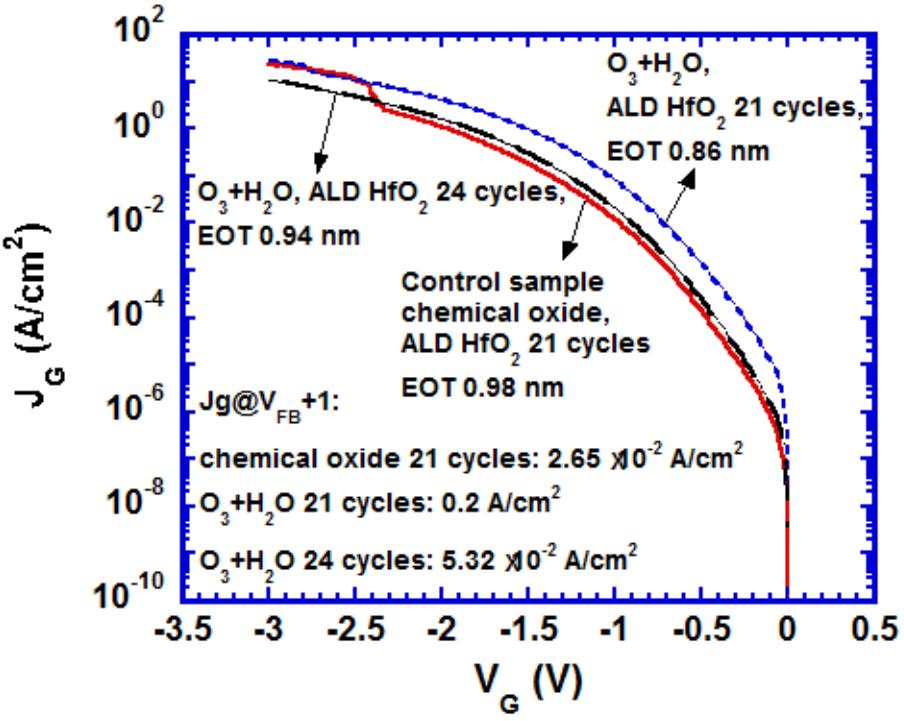


Figure 6.6. Leakage current density curves of the same MOS capacitors as shown in Figures 6.4 and 6.5.

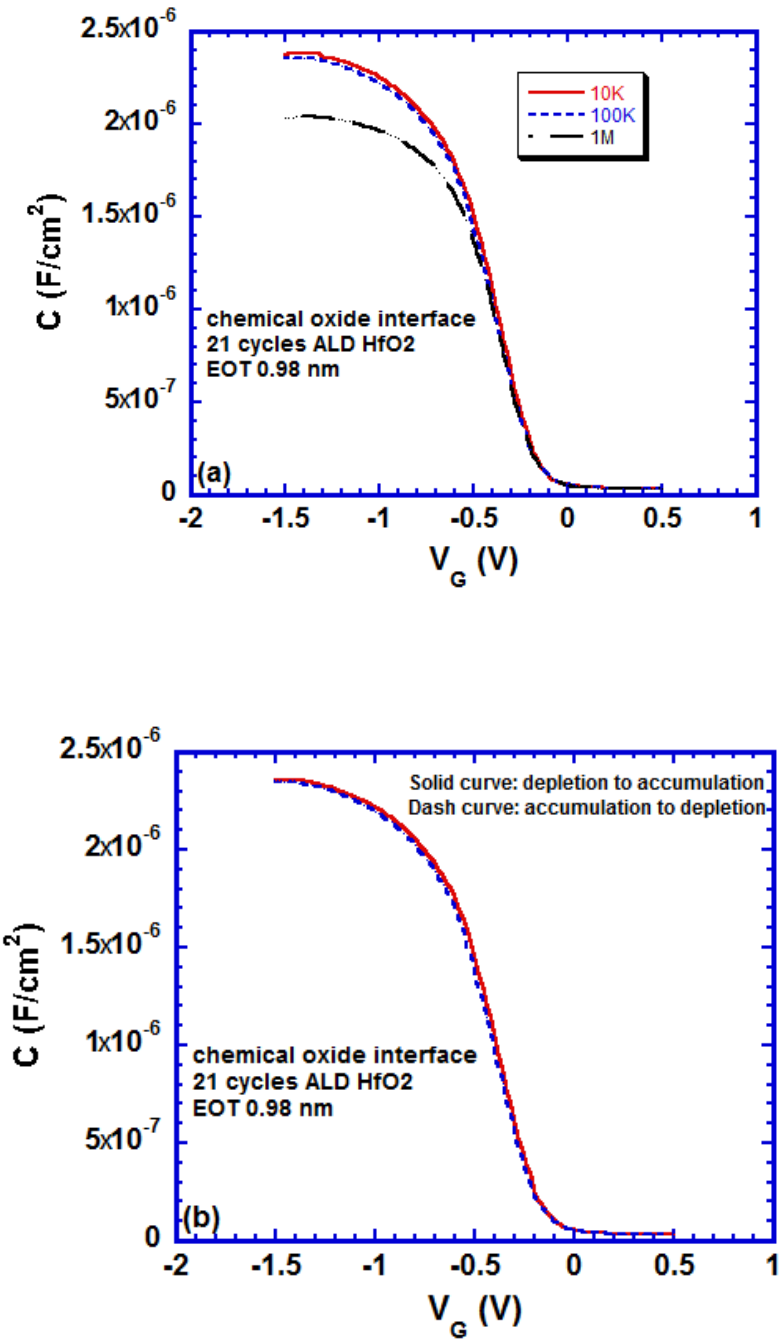


Figure 6.7. (a) Frequency dispersion (10 KHz, 100 KHz, 1 MHz) of C-V curve of MOS capacitor using chemical oxide/21-cycle-ALD HfO_2 as gate dielectric. (b) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in Figure 6.7(a).

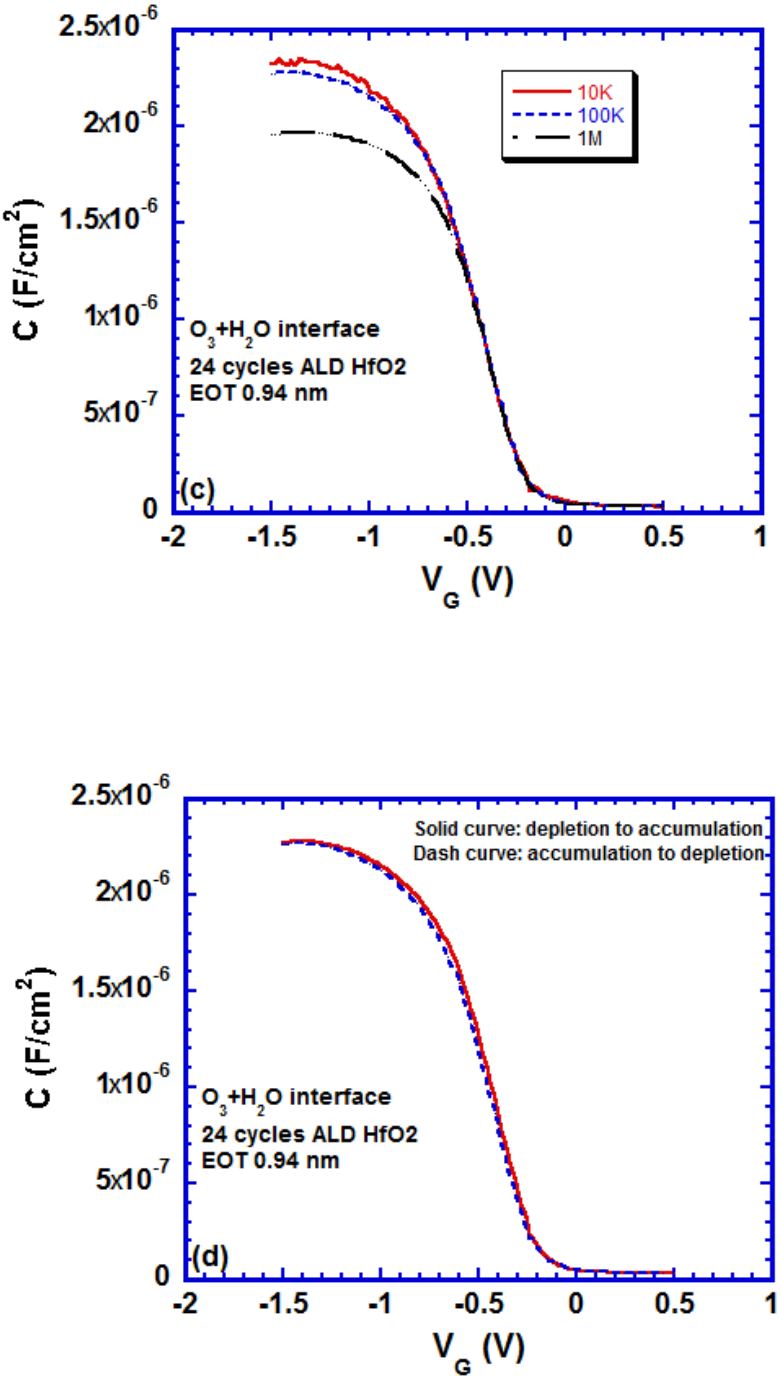


Figure 6.7. (c) Frequency dispersion (10 KHz, 100 KHz, 1 MHz) of C-V curve of MOS capacitor using ALD O_3+H_2O interface/24-cycle-ALD HfO_2 as gate dielectric. (d) Hysteresis behavior of 100 KHz C-V curve of the MOS capacitor in Figure 6.7(c).

Chapter 7 Atomic layer deposition of HfO_2 using HF etched thermal and RTP SiO_2 as interfacial layers

7.1 Introduction

Many methods were developed to prepare different interfacial layers for ALD of high-k dielectric materials, and the effectiveness of the interfacial layers were discussed in the publications. These interfacial layers include chemical oxide[1, 2], thermal SiO_2[1, 3], SiO_xN_y[1, 3], ozone oxide[3-6], etc. Among all these interfacial layers, chemical oxide is most widely used, and HfO_2 thin films grown on chemical oxide grown by SC1 solution (2 NH_4OH: 4 H_2O_2: 200 H_2O) has the best quality (See Chapter 5 for details). It was reported that thermal SiO_2 and Rapid Thermal Process (RTP)-grown SiO_2 are not good as interfacial layers because they are lack of –OH groups, and the ALD of HfO_2 on them faces a challenge of extra nucleation barrier, resulting in low HfO_2 coverage[1].

In this research, we proved that after controllable etching in diluted HF solution, thermal and RTP SiO_2 become highly hydrophilic on the surface, and can be used as interfacial layers for HfO_2 deposition. The electrical quality of HfO_2 is not degraded by these interfacial layers. We studied the physical and electrical properties of HfO_2 thin films deposited on thermal and RTP SiO_2 using ellipsometry measurement of HfO_2 films and electrical measurement of the metal-oxide-semiconductor (MOS) capacitors.

7.2 Experimental

Boron doped p-type Si(100) substrate with a resistivity of 1-20 Ω cm was used. The substrate was cleaned using Radio Corporation of America (RCA) cleaning to remove organic and ionic contaminations. After RCA cleaning, the substrate was cleaned using a BOE (buffered oxide etch) solution, providing an H-terminated surface of the silicon substrate. The surface was hydrophobic, which suggested that no oxide was left. The substrate was then loaded into quartz tube furnace for thermal oxidation. The thermal oxidation was executed at 900°C in diluted oxygen (O_2:N_2=1:5) for 20 seconds followed by a 20 minutes anneal, and a high quality ultrathin SiO_2 layer with thickness around 22Å was obtained (see Chapter 2 for details). After thermal oxidation, the substrate was cut into 2 pieces, one piece went through Rapid Thermal Process (RTP) at 1070°C for 2 minutes in helium and trace O_2. The temperature ramped up at a rate of 10°C/second, and the trace O_2 concentration was ~840 ppm (parts per million). The details of the RTP setup are described in Chapter 3. After RTP, the thickness of the thermal SiO_2 was increased by 5-6Å.

Aqueous hydrofluoric acid (HF, 49 wt %) was diluted using deionized water (DI water), and the volume ratio of aqueous HF to DI water is 3:1000. Both the thermal SiO_2 sample and the RTP SiO_2 sample were etched in the diluted HF solution. By controlling the etching time, the thicknesses of the SiO_2 thin films were reduced to 3.5-4.5Å, which is comparable to the thickness of chemical oxide used as an interfacial layer for ALD of high-k materials. It was found that although fresh thermal and RTP SiO_2 were lack of –OH groups and the surfaces are almost hydrophobic, the surfaces of the thin films turned into hydrophilic after wet etching in diluted HF solution. This phenomenon was also reported by G. Gould and

E. A. Irene[7]. The HF etched hydrophilic thermal oxide and RTP SiO_2 were used as interfacial layers for ALD of HfO_2.

The chemical oxide interfacial layer was also grown using SC 1 solution ($2NH_4OH$: $4H_2O_2$: 200 DI H_2O) at 60°C for 2 minutes, in order to provide a reference. The thickness of the chemical oxide was ~4.5Å. Detailed information about the chemical oxide as an interfacial layer has been studied before[8], and is illustrated in Chapter 5.

Using chemical oxide, HF etched thermal oxide, and HF etched RTP SiO_2 as interfacial layers, HfO_2 was deposited for 21 cycles using ALD (*Cambridge NanoTech Inc*) at 300°C. The precursors were tetrakis(dimethylamido)hafnium (TDMAH) and H_2O. Details of the HfO_2 deposition by ALD were described in Chapter 5. After deposition of HfO_2, multi-angle Spectroscopic Ellipsometry (*J. A. Woollam* M3000 V) was used to measure the physical thickness and optical constants (n-refractive index, and k-extinction coefficient) of the thin HfO_2 films. The physical thicknesses of the 21-cycle-ALD HfO_2 on different interfacial layers are consistent, and are around 30Å.

MOS capacitors were fabricated to characterize the electrical properties of the thin HfO_2 films and the interface quality. The metal gate stack was 100Å Titanium (Ti) covered by 1000Å Nickel (Ni), which were deposited by electron-beam evaporator. The metal gate was patterned by photolithography and wet etching, and the gate patterns were circles with diameter equals to 100 μm. The backside of the Si substrates was coated by 1000Å Aluminum (Al), which was also deposited by e-beam evaporation. The samples were

annealed at 450^{0}C in forming gas for 30 min., which created an Ohmic contact between Al and the bulk Si.

The capacitance-voltage (C-V) curves were measured using an Agilent 4284A LCR meter at different frequencies, and the current-voltage (I-V) curves were measured with an Agilent 4155B semiconductor parameter analyzer. Equivalent Oxide Thicknesses (EOT) and flatband voltages (V_{FB}) were extracted from the 100 KHz C-V curves by using theoretical quasi-static C-V simulation which took quantum mechanics into consideration.

7.3 Results and Discussion

7.3.1 Precisely controlled etch of thermal and RTP SiO_2 in diluted HF solution

In order to reduce the thermal and RTP SiO_2 thickness from 20-30Å to 3.5-4.5Å, we need to dilute HF solution to get proper etching rate. The concentrations of the HF solutions which are commonly used in semiconductor industry are too high and the ultrathin SiO_2 films would be totally etched out in several seconds[9, 10]. Concentrated HF reagent (49 wt %) was diluted with the volume ratio of HF to DI H_2O equals to 3:1000. In order to study the etch rate of high quality thermal SiO_2 in this solution, thick SiO_2 was thermally grown at 900°C in pure O_2 for 25 minutes, and the thickness of SiO_2 after oxidation was 162.26Å. The film thickness was measured by multi-angle spectroscopic ellipsomety with MSE around 5. This film was etched in diluted HF solution until the thickness was reduced to 4.03Å. During the etch process, the sample was taken out from the HF solution for measuring the remaining oxide thickness once for a while, in order to prevent over-etch. The details of the etch process are included in table 7.1. After etching in the diluted HF

solution for 5 minutes, the thickness of the SiO_2 film was reduced by 45.65Å, and the etch rate in the beginning 5 minutes was 9.13Å/min. This process was repeated 3 times for 5 minutes, 7 minutes and 2.5 minutes, until the thickness of the SiO_2 was reduced to 4.03Å, which is proper as an interfacial layer for ALD of HfO_2. The overall etch rate of thermal SiO_2 grown at 900°C in the diluted (3:1000) HF solution is 8-9Å/min.

Using the same method, extra data about the etch rates of various materials in the diluted (3:1000) HF solution were produced, and the results are listed in table 7.2. Various materials include native SiO_2, ALD SiO_2 after RTP, ALD HfO_2, and ALD HfO_2 after RTP. The etch rate of native SiO_2 is ~10Å/min, which is slightly higher than that of thermal SiO_2 grown at 900°C as stated above. This could be attributed to the relatively loose structure of the native SiO_2. The etch rate of the as deposited HfO_2 is ~10Å/min, and it is reduced to ~0Å/min after RTP. This implies the material property of the ALD HfO_2 could be significantly changed by RTP at 1050°C. In contrast, there was no observable difference between the etch rate of thermal SiO_2 and the etch rate of RTP SiO_2.

As stated in the Experimental Section, ~22Å-thermal SiO_2 and ~28Å-RTP SiO_2 (The thermal SiO_2 had ~6Å regrowth after RTP) were etched in dilute HF solution to reduce the thickness, such that they could be used as interfacial layers for ALD of HfO_2. Using the etch rates listed in table 7.1 as references, etch time was precisely controlled. The thickness of the thermal SiO_2 was reduced to ~3.5Å, and the thickness of the RTP SiO_2 was reduced to ~4.5Å.

7.3.2 Electrical characterization of HfO_2 thin films grown on different interfacial layers

21-cycle-ALD HfO_2 was grown on chemical oxide, HF etched thermal SiO_2 and HF etched RTP SiO_2. MOS capacitors were fabricated to characterize the electrical properties of the SiO_2/HfO_2 dielectric stacks. In order to have clear labels, the sample using chemical oxide as the interfacial layer is named Sample 1, the one using HF etched thermal SiO_2 as the interfacial layer is named Sample 2, and the one using HF etched RTP SiO_2 as the interfacial layer is named Sample 3. Figures 7.1 and 7.2 show the high frequency (100 KHz) Capacitance density-Voltage (C-V) curves of MOS capacitors using HF etched thermal and RTP SiO_2 as interfacial layers (Samples 2 and 3), and the C-V curves of the capacitors using chemical oxide as interfacial layer (Sample 1) are also plotted in both figures as a reference. The dots in the figures are the experimental C-V data (circles are data from the chemical oxide sample, triangles are data from the HF etched thermal SiO_2 sample, and squares are data from the HF etched RTP SiO_2 sample), and the solid curves are quasi-static simulations that takes quantum effects into consideration. Each of the experimental C-V data is a typical representative of the results of 10-15 measured devices. By fitting the theoretical C-V simulations with the experimental C-V data, we can extract the Equivalent Oxide Thicknesses (EOTs) and flatband voltages (V_{FB}) of the MOS capacitors. The fittings of the simulations to the measurement data are precise in the depletion region and in the initial part of the accumulation region, which implies the extraction of EOTs and V_{FB} is reliable. In the high-voltage part of the accumulation region, the capacitance densities drop, which introduce deformation to the measured C-V curves. This is because the interfacial

layer/21-cycle-ALD HfO_2 dielectric stacks are ultrathin, thus the direct tunneling current are high, which cause C-V deformation in the high gate voltage region[11].

The physical thickness of HfO_2 thin films on these 3 samples were 3.06 nm, 3.07 nm and 3.06 nm, separately, and the corresponding EOTs were 0.98 nm, 0.99 nm and 1.07 nm. Both the physical thicknesses and the EOTs of the 21-cycle-ALD HfO_2 grown on chemical oxide and HF etched thermal SiO_2 are the same, which suggests that the electrical quality of HfO_2 would not be harmed by using HF etched thermal SiO_2 as the interfacial layer. The remaining SiO_2 interfacial layer on the RTP SiO_2 sample (Sample 3) was thicker (~4.5Å) than that on the thermal SiO_2 sample (sample 2, ~3.5Å), which may explain why the EOT of sample 3 is ~1Å thicker than the EOTs of Samples 1 and 2. The V_{FB} are also marked in Figures 7.1 and 7.2, and will be used to evaluate the gate leakage current.

Figure 7.3 shows the Current density-Voltage (J-V) curves of the MOS capacitors on samples 1-3. The gate leakage current densities are evaluated at $V_G=V_{FB}+1V$, and they are listed in the Figure. The gate leakage current of Sample 1 at $V_G=V_{FB}+1V$ is 6×10^{-2} A/cm^2, which matches pretty well with the previously reported results[12, 13]. The gate leakage current of Sample 2 is 9.5×10^{-2} A/cm^2. The MOS capacitors using HF etched thermal SiO_2 interfacial layer has comparable gate leakage current to those using chemical-oxide interfacial layer, although there is a kink in the low voltage region of the J-V curve, which implies the interfacial quality is not ideal. We suggest that the remaining SiO_2 might be slightly damaged during the HF etch, so that a thicker interfacial layer might be needed for providing interfacial protection when using HF etched thermal SiO_2 as interfacial layer.

The gate leakage current of Sample 3 is the lowest one among those of all the three samples (3.7×10^{-2} A/cm^2), although it is still in the same order of magnitude (10^{-2} order) to the gate leakage current of the other two samples. This phenomenon corresponds to the thicker EOT of sample 3, and could also be attributed to the thicker interfacial layer on sample 3.

The gate leakage current density is controlled by the quality of the HfO_2 thin films, and the initial nucleation plays a key part in the growth of high quality HfO_2 using ALD. During the initial nucleation, molecules of TDMAH chemically attach to –OH groups on the surface of the interfacial layer. The interfacial layer should be hydrophilic with high –OH group density to provide sufficient sites for the TDMAH molecules to attach to. The gate leakage current of MOS capacitors using HF etched thermal and RTP SiO_2 as interfacial layers are comparable to that of MOS capacitors using chemical oxide as an interfacial layer, which suggests that the HF etched thermal and RTP SiO_2 could be used as effective interfacial layers.

7.3.3 The interfacial quality of ALD HfO_2 using different interfacial layers

In order to further study the effectiveness of HF etched thermal and RTP SiO_2 as interfacial layers for ALD of HfO_2, we measured the frequency dispersion of the C-V curves. Figure 7.4(a) shows the C-V curves of the MOS capacitor using chemical oxide as the interfacial layer (sample1), the C-V curves were measured at 10 KHz, 100 KHz and 1 MHz. The frequency dispersion of sample 1 is set as an interfacial quality reference. Figure 7.4(b) and (c) are the frequency dispersions of MOS capacitors using HF etched thermal SiO_2 and RTP SiO_2 as interfacial layers. The Figures 7.4(a), (b) and (c) exhibit similar C-V

frequency dispersion behavior: the C-V curves measured at different frequency overlap with each other in depletion region, the V_{FB} value would be the same when extracted from each C-V curve, and the 1 MHz C-V curve has lower accumulation capacitance comparing to the 10 KHz and 100 KHz C-V curves. The consistent V_{FB} suggests there is no C-V frequency dispersion in all the three samples, and the interfacial quality is good. The dropped capacitance density in the accumulation region of the 1 MHz C-V curve is caused by the series resistance of the gate electrodes[14-16].

Figure 7.5(a), (b) and (c) show the hysteresis behavior of MOS capacitors using chemical oxide, HF etched thermal SiO_2 and HF etched RTP SiO_2 as interfacial layers. The C-V curves were measured at 100 KHz. The solid curves were measured from depletion to accumulation, and the dash curves were measured from accumulation to depletion. In Figure 7.5(a), (b) and (c), the two C-V curves in each figure overlap with each other, and the V_{FB} extracted from each curve would be almost the same. This suggests the C-V hysteresis is negligible, and the mobile charge amount in the dielectric stack is small. In Figures 7.5(a) and 5(b), we can barely recognize the dash curve from the solid curve, while in Figure 7.5(c), it is even more difficult to tell the two curves. The hysteresis behavior of the HF etched RTP SiO_2 sample is even better, and this could be attribute to the good interfacial quality between the Si substrate and the SiO_2 interfacial layer after RTP.

Based on the analysis above, The C-V frequency dispersion and hysteresis behavior of Samples 2 and 3 are all negligible and comparable to Sample 1, which suggest that the

interfacial quality of ALD HfO_2 is not degraded when using HF etched thermal and RTP SiO_2 as interfacial layers.

In Chapter 3, we discussed the formation of a strained Si layer at the SiO_2/Si interface after the rapid heating up and cooling down process in the RTP. However, in the situation of this chapter, it is likely that the strain of the interfacial Si would be released during the diluted HF etching. Plus, p-type Si substrates were used in this chapter, and it was discussed in Chapter 3 that the valence band E_v of the strained Si remains unaltered. As a result, the leakage current reduction phenomenon was observed in the high-k gate dielectric based MOS capacitors discussed in this chapter.

7.4 Conclusion

In summary, diluted HF etch of thermal and RTP SiO_2 creates hydrophilic surfaces, which can be used as interfacial layers for ALD of HfO_2. The EOT, gate leakage current, and interfacial quality of the HfO_2 are comparable to those of the HfO_2 grown on chemical oxide. This may provide a new way for interfacial oxide preparation for ALD HfO_2 growth.

Table 7.1. Etch rate of thermal SiO_2 grown at 900°C in diluted (3:1000) HF solution. The mean squared errors (MSEs) of the spectroscopic ellipsometry measurements are < 5.

Etch time	**Start thickness**	**End thickness**	**ΔThickness**	**Etch rate**	
5 min	162.26Å	116.61Å	45.65Å	9.13Å/min	**Average etch rate** 8.11Å/min
5 min	116.61Å	75.23Å	41.38Å	8.28Å/min	
7 min	75.23Å	25.41Å	49.82Å	7.12Å/min	
2.5 min	25.41Å	4.03Å	21.38Å	8.55Å/min	

Table 7.2. Approximate etch rates of various materials in diluted (3:1000) HF solution.

Material	**Approximate etch rate**
Native SiO_2	~10Å/min
ALD SiO_2 after RTP at 1050°C for 1 min	~2Å/min
ALD HfO_2	~10Å/min
ALD HfO_2 after RTP at 1050°C for 1 min	~0Å/min

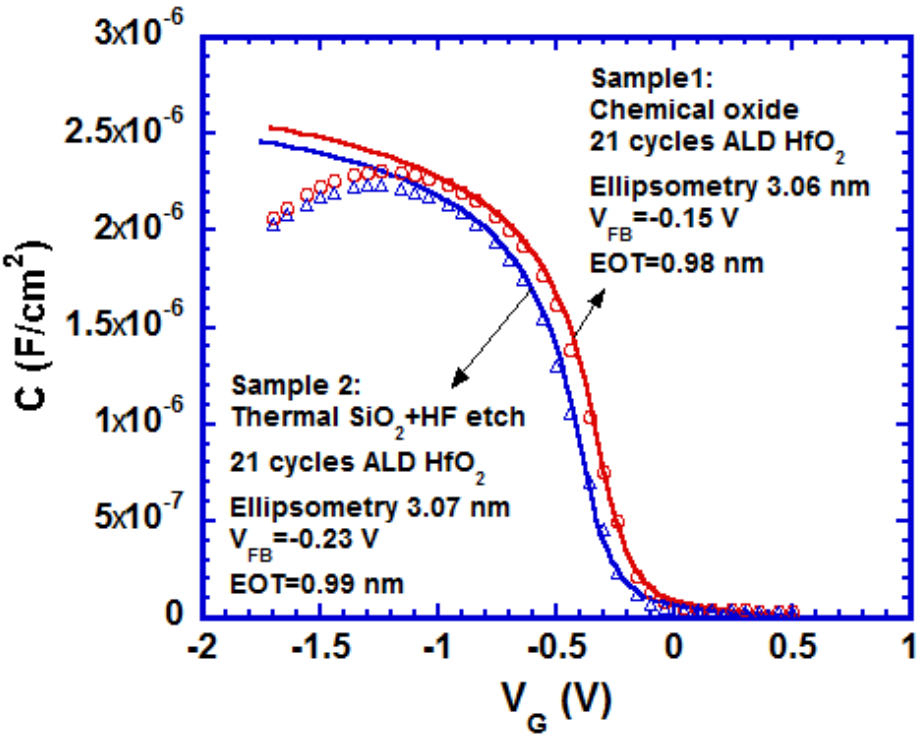


Figure 7.1. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The experimental C-V curves were measured at 100 KHz. The interfacial layers were formed by SC1 chemical oxidation (Sample 1), and by thermal oxidation+HF etching (Sample 2). The HfO_2 were deposited using ALD for 21 cycles.

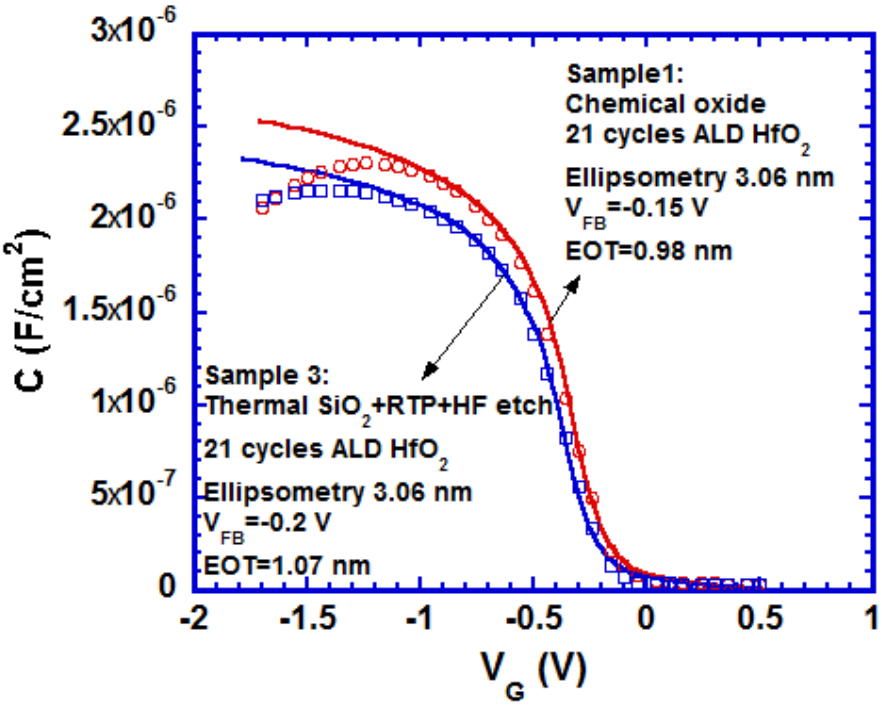


Figure 7.2. Experimental (dots) and simulated (lines) C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The interfacial layers were formed by SC1 chemical oxidation (Sample 1) and by RTP oxidation+HF etching (Sample3). The HfO_2 were deposited using ALD for 21 cycles.

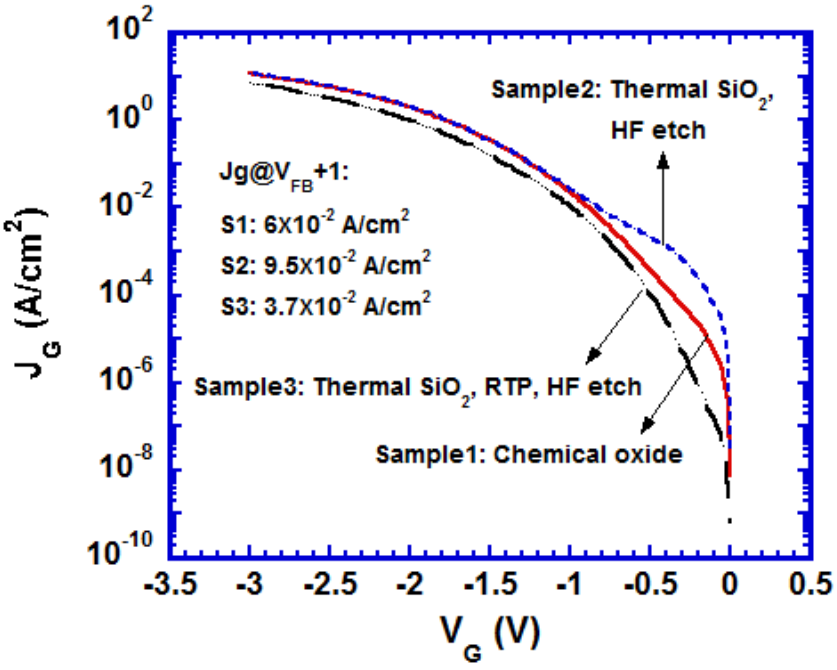


Figure 7.3. Leakage current density curves of the MOS capacitors in Figures 7.1 and 7.2.

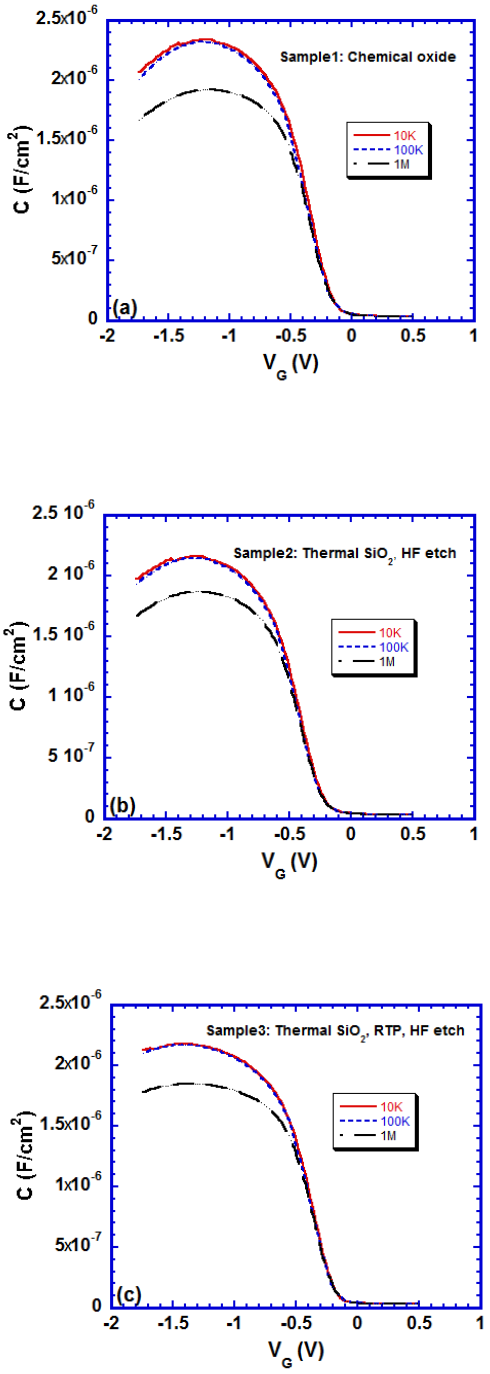


Figure 7.4. Frequency dispersion (10 KHz, 100 KHz, 1 MHz) of C-V curves of Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The HfO_2 was deposited using ALD for 21 cycles. The interfacial layers are (a) chemical oxide; (b) HF etched thermal SiO_2; (c) HF etched RTP SiO_2.

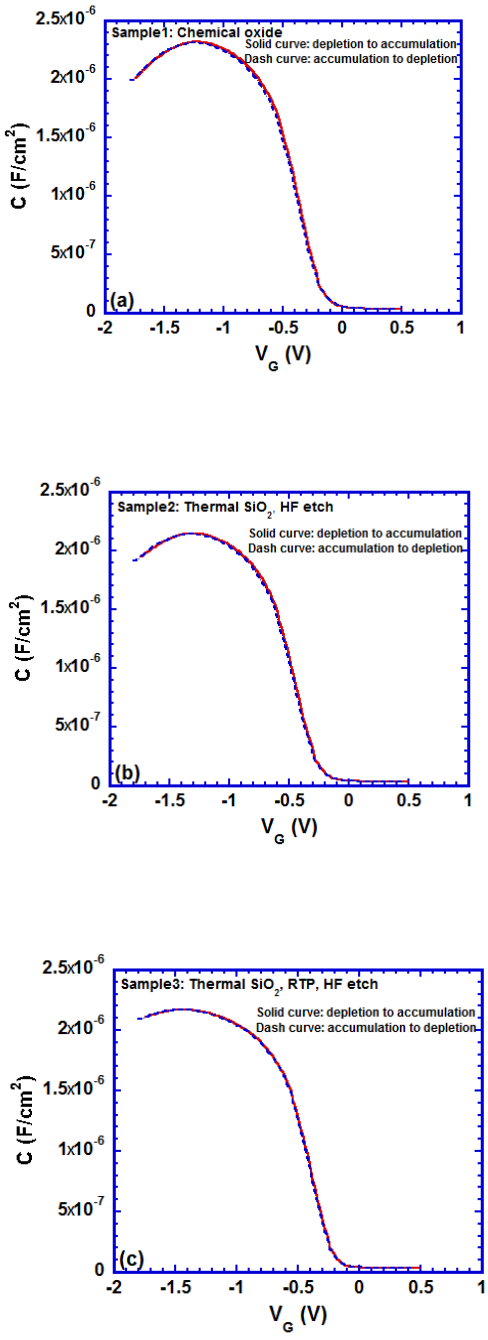


Figure 7.5. Hysteresis behavior of 100 KHz C-V curves of the Ni/Ti/HfO_2/interfacial layer/p-Si MOS capacitors. The HfO_2 was deposited using ALD for 21 cycles. The interfacial layers are (a) chemical oxide; (b) HF etched thermal SiO_2; (c) HF etched RTP SiO_2.

Chapter 8 Conclusion and Future Work

8.1 Conclusion

The continuous shrink of the semiconductor device dimensions is approaching the limitation, and the innovations of the materials and structures are urgently needed in the MOS devices, in order to meet the performance expectation of the integrated circuits (IC). HfO_2 has replaced SiO_2 and became the mainstream gate dielectric, while SiO_2 is still needed in many cases. Investigations of the gate dielectric materials and the dielectric/silicon interfaces were presented in this dissertation.

Using a RTP based lateral heating treatment, the gate leakage current of the ultrathin thermal SiO_2 based MOS capacitors was reduced by 4-5 orders of magnitude. The appealing electrical property of the MOS capacitors was attributed to the structure change of the Si at the SiO_2/Si interface after the lateral heating treatment. A thin layer of strained Si with tensile stress was formed due to the rapid heating up and cooling down process. The conduction band E_c of the strained Si layer is decreased, and the valence band E_v is unaltered. The potential barrier height between the interfacial Si and the SiO_2 is increased, resulting the direct tunneling current reduction.

High quality SiO_2 thin films were grown by ALD. Excellent linearity for growth was observed. The growth rate increased at higher temperatures. When EOT <3.5 nm, the ALD SiO_2 has gate leakage current density comparable to that of thermal SiO_2 grown at temperatures above 800^0C. The frequency dispersion and hysteresis behavior of the C-V

curves of the ALD SiO_2 films deposited at 100°C, 200^{0}C, and 300^{0}C are all very small in the thickness region of <3.5 nm, suggesting excellent interfacial quality. Based on analysis of mismatch between the films' EOT and their physical thicknesses, the ALD SiO_2 thin films are likely to be silicon-rich in composition. At the deposition temperature of 100°C and for thickness <3.5 nm, which is important to thin-film MOS transistors, the EOT-based breakdown electrical fields (~10MV/m) of ALD SiO_2 are nearly as good as that of thermal SiO_2, and the physical thickness-based breakdown electric-fields (~8MV/cm) are slightly worse than that of thermal SiO_2, although the thin films contain more H impurity than thermal silicon oxide. At deposition temperatures of 200°C and 300°C, the EOT-based breakdown e-fields (9-10MV/cm) of ALD SiO_2 are close to that of the thermal SiO_2 and the physical thickness-based breakdown e-fields (5-8MV/cm) are worse than that of thermal SiO_2. At all deposition temperatures, the ultrathin ALD SiO_2 (<3.5nm) has both excellent EOT- and physical thickness-based breakdown e-fields (~10MV/cm), which are almost comparable to that of thermal SiO_2. The appealing electrical properties of thin ALD SiO_2 (<3.5 nm) enable its potential applications as high-quality gate insulators for thin-film MOS transistors, and insulators for sensor structures and nanostructures on non-silicon substrates.

High quality HfO_2 thin film was grown by ALD, and the interface condition was extensively investigated. Chemical oxide grown by SC 1 solution has been proved to be an effective interfacial layer. 4.5 Å is the minimum thickness needed for the chemical oxide to be a high quality interface. Using the chemical oxide as a reference, 2 innovative interfacial layers were developed. The first interfacial layer was grown by in-situ ozone

and H_2O exposure in the ALD chamber. Multi-angle spectroscopic ellipsometry and XPS were used to characterize the interfacial layer. Studies of HfO_2 growth linearity, EOT of the stack, gate leakage current, and frequency dispersion and hysteresis behavior of the C-V curves suggest that the in-situ formed interfacial layer can result in the same high-quality HfO_2 dielectric layer as the chemical oxide interfacial layer. Using this approach, the wet chemical oxidation step can be eliminated from the processes of deposition of high-k gate stacks, which is economically beneficial to the industry. The second interfacial layer was prepared by controllable etching of thermal and RTP SiO_2 in diluted hydrofluoric acid (HF) solution. The EOT, gate leakage current, and interfacial quality of the HfO_2 are comparable to those of the HfO_2 grown on chemical oxide. This may provide a new way for interfacial oxide formation for ALD HfO_2 growth.

8.2 Future work

Following the development trend of the semiconductor industry, further research is needed as listed below.

ITRS has raised the urgent needs for dielectric materials with k values higher than that of HfO_2 (k>30), namely higher-k dielectric materials, in order to further support the scaling[1]. Two innovative SiO_2-like interfacial layers were developed in this dissertation, and the effectiveness of the interfacial layers for higher-k dielectric materials needs to be studied. Incompatibility between the interfacial layers and the higher-k dielectric materials would result in growth incubation period, increase of interface states, and degradation of the material and electrical properties of the higher-k materials. These issues must be studied

before implementing the interfacial layers for the higher-k dielectric materials based transistors.

Germanium (Ge) and III-V materials have high carrier mobility, and are expected to replace Si to form the conductive channel and promote the performance of transistors. The control of the interface states is a key challenge which prohibits the application of the high mobility materials. Abundant interface states at the channel/gate oxide interface would enhance the carrier scattering effect, decreasing carrier mobility and leading to malfunction of transistors. The ultrathin ALD SiO_2 films have the potential to be used as the passivation layers for the high mobility materials. The interfacial quality between ALD SiO_2 and high mobility materials is essential and must be characterized in details.

Additional, the effectiveness of ALD SiO_2 films as the interfacial layers for growth of high-k dielectric oxides should be studied. It was reported that –OH groups terminated SiO_2 surface could be achieved by introducing H_2O into the ALD cycle[2]. The material and electrical properties of the –OH groups terminated SiO_2, as well as the high-k dielectric oxides grown using the SiO_2 as the interfacial layer, worth to be studied in depth. The study should be based on both Si and high mobility materials.

Reference

Chapter 1

[1] I. PRESENT, "Cramming more components onto integrated circuits," *Readings in computer architecture,* p. 56, 2000.

[2] G. D. Wilk, R. M. Wallace, and J. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *Journal of applied physics,* vol. 89, pp. 5243-5275, 2001.

[3] T. Hori, *Gate dielectrics and MOS ULSIs*: Springer, 1997.

[4] J. Singh, *Semiconductor devices: basic principles*: John Wiley & Sons, 2007.

[5] A. Brand, "Precision materials to meet scaling challenges beyond 14nm " in *Semicon West 2013*, 2013.

[6] L. Colombo, J. Chambers, and H. Niimi, "gate Dielectric Process technology for the sub-1 nm equivalent Oxide thickness (eOt) era," *INTERFACE-PENNINGTON-,* vol. 16, p. 51, 2007.

[7] S. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *Electron Device Letters, IEEE,* vol. 18, pp. 209-211, 1997.

[8] M. Cao, P. Vande Voorde, M. Cox, and W. Greene, "Boron diffusion and penetration in ultrathin oxide with poly-Si gate," *Electron Device Letters, IEEE,* vol. 19, pp. 291-293, 1998.

[9] H. Tuinhout, A. Montree, J. Schmitz, and P. Stolk, "Effects of gate depletion and boron penetration on matching of deep submicron CMOS transistors," in *International electron devices meeting*, 1997, pp. 631-634.

[10] M. Fischetti and S. Laux, "Performance degradation of small silicon devices caused by long-range Coulomb interactions," *Applied Physics Letters,* vol. 76, pp. 2277-2279, 2000.

[11] G. Timp, A. Agarwal, F. Baumann, T. Boone, M. Buonanno, R. Cirelli*, et al.*, "Low leakage, ultra-thin gate oxides for extremely high performance sub-100 nm nMOSFETs," in *Electron Devices Meeting, 1997. IEDM'97. Technical Digest., International*, 1997, pp. 930-932.

[12] S. I. Association, "International Technology Roadmap for Semiconductors, 2013 edition," 2013.

[13] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Reports on Progress in Physics,* vol. 69, p. 327, 2006.

[14] W. B. Blumenthal, *The chemical behavior of zirconium*: van Nostrand, 1958.

[15] O. Engström, B. Raeissi, S. Hall, O. Buiu, M. C. Lemme, H. Gottlob*, et al.*, "Navigation aids in the search for future high-k dielectrics: Physical and electrical trends," *Solid-State Electronics,* vol. 51, pp. 622-626, 2007.

[16] L. Manchanda, W. Lee, J. Bower, F. Baumann, W. Brown, C. Case*, et al.*, "Gate quality doped high K films for CMOS beyond 100 nm: 3-10 nm Al/sub 2/O/sub 3/with low leakage and low interface states," in *Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International*, 1998, pp. 605-608.

[17] S. Chen, C. Lai, A. Chin, J. Hsieh, and J. Liu, "High-density MIM capacitors using Al 2 O 3 and AlTiO x dielectrics," *Electron Device Letters, IEEE,* vol. 23, pp. 185-187, 2002.

[18] D.-G. Park, H.-J. Cho, C. Lim, I.-S. Yeo, J.-S. Roh, C.-T. Kim*, et al.*, "Characteristics of Al/sub 2/O/sub 3/gate dielectric prepared by atomic layer deposition for giga scale CMOS DRAM devices," in *VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on*, 2000, pp. 46-47.

[19] M. Copel, E. Cartier, E. Gusev, S. Guha, N. Bojarczuk, and M. Poppeller, "Robustness of ultrathin aluminum oxide dielectrics on Si (001)," *Applied Physics Letters,* vol. 78, pp. 2670-2672, 2001.

[20] S. Guha, E. Gusev, H. Okorn-Schmidt, M. Copel, L.-A. Ragnarsson, N. Bojarczuk*, et al.*, "High temperature stability of Al 2 O 3 dielectrics on Si: Interfacial metal diffusion and mobility degradation," *Applied Physics Letters,* vol. 81, pp. 2956-2958, 2002.

[21] C.-Y. Lin, C.-Y. Wu, C.-Y. Wu, C. Hu, and T.-Y. Tseng, "Bistable resistive switching in Al2O3 memory thin films," *Journal of The Electrochemical Society,* vol. 154, pp. G189-G192, 2007.

[22] S. Nakata, K. Saito, and M. Shimada, "Nonvolatile memory using Al 2 O 3 film with an embedded Al-rich layer," *Applied Physics Letters,* vol. 87, pp. 223110-223110-3, 2005.

[23] C. H. Shin, S. Y. Cha, H. C. Lee, W.-J. Lee, B.-G. Yu, and D.-H. Kwak, "Fabrication and characterization of MFISFET using Al2O3 insulating layer for non-volatile memory," *Integrated Ferroelectrics,* vol. 34, pp. 113-120, 2001.

[24] C.-H. Lee, S.-H. Hur, Y.-C. Shin, J.-H. Choi, D.-G. Park, and K. Kim, "Charge-trapping device structure of SiO 2/SiN/high-k dielectric Al 2 O 3 for high-density flash memory," *Applied Physics Letters,* vol. 86, pp. 152908-152908-3, 2005.

[25] O. Buiu, S. Hall, O. Engstrom, B. Raeissi, M. Lemme, P. Hurley*, et al.*, "Extracting the relative dielectric constant for "high-κ layers" from CV measurements–Errors and error propagation," *Microelectronics Reliability,* vol. 47, pp. 678-681, 2007.

[26] S. Hall, O. Buiu, I. Z. Mitrovic, Y. Lu, and W. M. Davey, "Review and perspective of high-k dielectrics on silicon," *Journal of Telecommunications and Information Technology,* pp. 33-43, 2007.

[27] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *Journal of Vacuum Science & Technology B,* vol. 18, pp. 1785-1791, 2000.

[28] K. F. Schuegraf and C. Hu, "Hole injection SiO 2 breakdown model for very low voltage lifetime extrapolation," *Electron Devices, IEEE Transactions on,* vol. 41, pp. 761-767, 1994.

[29] M. Lenzlinger and E. Snow, "Fowler‐Nordheim Tunneling into Thermally Grown SiO2," *Journal of Applied physics,* vol. 40, pp. 278-283, 1969.

[30] A. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultra-thin gate dielectrics," *Journal of applied physics,* vol. 81, pp. 7900-7908, 1997.

[31] E. Bersch, S. Rangan, R. A. Bartynski, E. Garfunkel, and E. Vescovo, "Band offsets of ultrathin high-κ oxide films with Si," *Physical Review B,* vol. 78, p. 085114, 2008.

[32] S. Miyazaki, "Photoemission study of energy-band alignments and gap-state density distributions for high-k gate dielectrics," *Journal of Vacuum Science & Technology B,* vol. 19, pp. 2212-2216, 2001.

[33] J.-H. Hong, T.-H. Moon, and J.-M. Myoung, "Microstructure and characteristics of the HfO 2 dielectric layers grown by metalorganic molecular beam epitaxy," *Microelectronic engineering,* vol. 75, pp. 263-268, 2004.

[34] J. Huang, D. Heh, P. Sivasubramani, P. Kirsch, G. Bersuker, D. Gilmer*, et al.*, "Gate first high-k/metal gate stacks with zero SiO x interface achieving EOT= 0.59 nm for 16nm application," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 34-35.

[35] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank*, et al.*, "Extremely scaled gate-first high-k/metal gate stack with EOT of 0.55 nm using novel interfacial layer scavenging techniques for 22nm technology node and beyond," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 138-139.

[36] T. Ando, M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken*, et al.*, "Understanding mobility mechanisms in extremely scaled HfO 2 (EOT 0.42 nm) using remote interfacial layer

scavenging technique and V t-tuning dipoles with gate-first process," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[37] M. Gutowski, J. E. Jaffe, C.-L. Liu, M. Stoker, R. I. Hegde, R. S. Rai*, et al.*, "Thermodynamic stability of high-k dielectric metal oxides ZrO 2 and HfO 2 in contact with Si and SiO 2," *Applied Physics Letters,* vol. 80, pp. 1897-1899, 2002.

[38] C. Lee, H. Luan, W. Bai, S. Lee, T. Jeon, Y. Senzaki*, et al.*, "MOS characteristics of ultra thin rapid thermal CVD ZrO/sub 2/and Zr silicate gate dielectrics," in *Electron Devices Meeting, 2000. IEDM'00. Technical Digest. International*, 2000, pp. 27-30.

[39] E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha*, et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 20.1. 1-20.1. 4.

[40] H. Kato, T. Nango, T. Miyagawa, T. Katagiri, K. S. Seol, and Y. Ohki, "Plasma-enhanced chemical vapor deposition and characterization of high-permittivity hafnium and zirconium silicate films," *Journal of applied physics,* vol. 92, pp. 1106-1111, 2002.

[41] W.-J. Qi, R. Nieh, B. H. Lee, K. Onishi, L. Kang, Y. Jeon*, et al.*, "Performance of MOSFETs with ultra thin ZrO/sub 2/and Zr silicate gate dielectrics," in *VLSI Technology, 2000. Digest of Technical Papers. 2000 Symposium on*, 2000, pp. 40-41.

[42] K. Kakushima, K. Tachi, M. Adachi, K. Okamoto, S. Sato, J. Song*, et al.*, "Interface and electrical properties of La-silicate for direct contact of high-k with silicon," *Solid-State Electronics,* vol. 54, pp. 715-719, 2010.

[43] R. Beyers, "Thermodynamic considerations in refractory metal ‐ silicon ‐ oxygen systems," *Journal of applied physics,* vol. 56, pp. 147-152, 1984.

[44] K. Hubbard and D. Schlom, "Thermodynamic stability of binary oxides in contact with silicon," *Journal of Materials Research,* vol. 11, pp. 2757-2776, 1996.

[45] C. Choi, C. Y. Kang, S. J. Rhee, M. S. Abkar, S. A. Krishna, M. Zhang*, et al.*, "Fabrication of TaN-gated ultra-thin MOSFETs (EOT< 1.0 nm) with HfO/sub 2/using a novel oxygen scavenging process for sub 65 nm application," in *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, 2005, pp. 226-227.

[46] K. Cherkaoui, S. Monaghan, M. Negara, M. Modreanu, P. Hurley, D. O'Connell*, et al.*, "Electrical, structural, and chemical properties of HfO2 films formed by electron beam evaporation," *Journal of Applied Physics,* vol. 104, p. 064113, 2008.

[47] B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters,* vol. 76, pp. 1926-1928, 2000.

[48] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, K. Tsu-Jae, J. Bokor*, et al.*, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *Electron Device Letters, IEEE,* vol. 21, pp. 254-255, 2000.

[49] J. Colinge, "Fully-depleted SOI CMOS for analog applications," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 1010-1016, 1998.

[50] D. Hisamoto, "FD/DG-SOI MOSFET-a viable approach to overcoming the device scaling limit," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 19.3. 1-19.3. 4.

[51] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo*, et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on,* vol. 47, pp. 2320-2325, 2000.

[52] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski*, et al.*, "Sub 50-nm FinFET: PMOS," in *Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International*, 1999, pp. 67-70.

[53] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang*, et al.*, "FinFET scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM'02. International*, 2002, pp. 251-254.

[54] C. Hu, T.-J. King, V. Subramanian, L. Chang, X. Huang, Y.-K. Choi*, et al.*, "Finfet transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture," ed: Google Patents, 2002.

[55] N. Singh, A. Agarwal, L. Bera, T. Liow, R. Yang, S. Rustagi*, et al.*, "High-performance fully depleted silicon nanowire (diameter$\leqslant$ 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.

[56] S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller*, et al.*, "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[57] J. Gu, Y. Liu, Y. Wu, R. Colby, R. G. Gordon, and P. D. Ye, "First experimental demonstration of gate-all-around III–V MOSFETs by top-down approach," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 33.2. 1-33.2. 4.

[58] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost*, et al.*, "A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193nm dry patterning, and 100% Pb-free packaging," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 247-250.

[59] R. L. Puurunen, "A short history of atomic layer deposition: Tuomo suntola's atomic layer epitaxy," *Chemical Vapor Deposition,* vol. 20, pp. 332-344, 2014.

[60] M. Leskelä and M. Ritala, "Atomic layer deposition chemistry: recent developments and future challenges," *Angewandte Chemie International Edition,* vol. 42, pp. 5548-5554, 2003.

[61] S. M. George, "Atomic layer deposition: an overview," *Chemical reviews,* vol. 110, pp. 111-131, 2009.

[62] J. Aarik, A. Aidla, A.-A. Kiisler, T. Uustare, and V. Sammelselg, "Influence of substrate temperature on atomic layer growth and properties of HfO 2 thin films," *Thin Solid Films,* vol. 340, pp. 110-116, 1999.

[63] X. Liu, S. Ramanathan, A. Longdergan, A. Srivastava, E. Lee, T. E. Seidel*, et al.*, "ALD of hafnium oxide thin films from tetrakis (ethylmethylamino) hafnium and ozone," *Journal of The Electrochemical Society,* vol. 152, pp. G213-G219, 2005.

[64] A. Deshpande, R. Inman, G. Jursich, and C. Takoudis, "Atomic layer deposition and characterization of hafnium oxide grown on silicon from tetrakis (diethylamino) hafnium and water vapor," *Journal of Vacuum Science & Technology A,* vol. 22, pp. 2035-2040, 2004.

[65] J. Niinistö, M. Putkonen, L. Niinistö, K. Arstila, T. Sajavaara, J. Lu*, et al.*, "HfO2 films grown by ALD using cyclopentadienyl-type precursors and H2O or O3 as oxygen source," *Journal of The Electrochemical Society,* vol. 153, pp. F39-F45, 2006.

[66] H. B. Park, M. Cho, J. Park, S. W. Lee, C. Seong Hwang, J.-P. Kim*, et al.*, "Comparison of HfO 2 films grown by atomic layer deposition using HfCl 4 and H 2 O or O 3 as the oxidant," *Journal of applied physics,* vol. 94, pp. 3641-3647, 2003.

[67] R. L. Puurunen, "Analysis of hydroxyl group controlled atomic layer deposition of hafnium dioxide from hafnium tetrachloride and water," *Journal of applied physics,* vol. 95, pp. 4777-4786, 2004.

[68] P. Kirsch, M. Quevedo-Lopez, H. Li, Y. Senzaki, J. Peterson, S. Song*, et al.*, "Nucleation and growth study of atomic layer deposited HfO 2 gate dielectrics resulting in improved

scaling and electron mobility," *Journal of applied physics,* vol. 99, pp. 023508-023508-8, 2006.

[69] J. C. Hackley, J. D. Demaree, and T. Gougousi, "Growth and interface of HfO 2 films on H-terminated Si from a TDMAH and H 2 O atomic layer deposition process," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 26, pp. 1235-1240, 2008.

[70] J. C. Hackley, T. Gougousi, and J. D. Demaree, "Nucleation of HfO2 atomic layer deposition films on chemical oxide and H-terminated Si," *Journal of Applied Physics,* vol. 102, p. 034101, 2007.

Chapter 2

[1] E. H. Nicollian, J. R. Brews, and E. H. Nicollian, *MOS (metal oxide semiconductor) physics and technology* vol. 1987: Wiley New York et al., 1982.

[2] W. Kern, "Cleaning solutions based on hydrogen peroxide for use in silicon semiconductor technology," *RCA review,* vol. 31, pp. 187-206, 1970.

[3] W. Kern, "Handbook of semiconductor wafer cleaning technology," *New Jersey: Noyes Publication,* pp. 111-196, 1993.

[4] B. E. Deal and A. Grove, "General relationship for the thermal oxidation of silicon," *Journal of Applied Physics,* vol. 36, pp. 3770-3778, 1965.

[5] Z. Chen, "Mechanism for generation of the phonon-energy-coupling enhancement effect for ultrathin oxides on silicon," *Applied Physics Letters,* vol. 91, pp. 223513-223513-3, 2007.

[6] Z. Chen and J. Guo, "Dramatic enhancement of phonon energy coupling at the SiO2/Si interface due to Rapid Thermal Processing of the gate oxide," in *35th IEEE Semiconductor Interface Specialists Conf*, 2004.

[7] Z. Chen and J. Guo, "Dramatic reduction of gate leakage current of ultrathin oxides through oxide structure modification," *Solid-state electronics,* vol. 50, pp. 1004-1011, 2006.

[8] Z. Chen, J. Guo, and F. Yang, "Phonon-energy-coupling enhancement: Strengthening the chemical bonds of the SiO 2/Si system," *Applied physics letters,* vol. 88, pp. 082905-082905-3, 2006.

[9] P.-L. Ong, Z. Chen, A. Haggag, and T.-Y. Luo, "Large leakage-current reduction of ultrathin industrial SiON wafers induced by phonon-energy-coupling enhancement," *Electrochemical and Solid-State Letters,* vol. 11, pp. H293-H295, 2008.

[10] Z. Chen, P.-L. Ong, and Y. Wang, "Reliable Observation of Large Leakage-Current Reduction of Thin SiO2 Induced by Phonon-Energy-Coupling Enhancement: Problems and Solution," *Journal of The Electrochemical Society,* vol. 157, pp. G44-G48, 2010.

[11] K. R. Williams, K. Gupta, and M. Wasilik, "Etch rates for micromachining processing-Part II," *Microelectromechanical Systems, Journal of,* vol. 12, pp. 761-778, 2003.

[12] R. H. Blick, F. Monzon, W. Wegscheider, M. Bichler, F. Stern, and M. Roukes, "Magnetotransport measurements on freely suspended two-dimensional electron gases," *Physical Review B,* vol. 62, p. 17103, 2000.

[13] Y. Wang, X. Chen, Y. Zhong, F. Zhu, and K. P. Loh, "Large area, continuous, few-layered graphene as anodes in organic photovoltaic devices," *Applied Physics Letters,* vol. 95, p. 063302, 2009.

Chapter 3

[1] E. Gusev, C. Cabral Jr, M. Copel, C. D'Emic, and M. Gribelyuk, "Ultrathin HfO< sub> 2</sub> films grown on silicon by atomic layer deposition for advanced gate dielectrics applications," *Microelectronic Engineering,* vol. 69, pp. 145-151, 2003.

[2] M.-Y. Ho, H. Gong, G. Wilk, B. Busch, M. Green, P. Voyles*, et al.*, "Morphology and crystallization kinetics in HfO2 thin films grown by atomic layer deposition," *Journal of Applied Physics,* vol. 93, pp. 1477-1481, 2003.

[3] H. Kim, P. C. McIntyre, and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO2 dielectrics grown by atomic layer deposition," *Applied physics letters,* vol. 82, pp. 106-108, 2003.

[4] Y. Morita, A. Hirano, S. Migita, H. Ota, T. Nabatame, and A. Toriumi, "Impact of Surface Hydrophilicization prior to Atomic Layer Deposition for HfO2/Si Direct-Contact Gate Stacks," *Applied physics express,* vol. 2, p. 011201, 2009.

[5] W. Tsai, R. Carter, H. Nohira, M. Caymax, T. Conard, V. Cosnier*, et al.*, "Surface preparation and interfacial stability of high-k dielectrics deposited by atomic layer chemical vapor deposition," *Microelectronic Engineering,* vol. 65, pp. 259-272, 2003.

[6] Z. Chen, "Mechanism for generation of the phonon-energy-coupling enhancement effect for ultrathin oxides on silicon," *Applied Physics Letters,* vol. 91, pp. 223513-223513-3, 2007.

[7] S. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *Electron Device Letters, IEEE,* vol. 18, pp. 209-211, 1997.

[8] B. Brar, G. Wilk, and A. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin SiO2," *Applied physics letters,* vol. 69, pp. 2728-2730, 1996.

[9] H. Sasaki, M. Ono, T. Yoshitomi, T. Ohguro, S.-i. Nakamura, M. Saito*, et al.*, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 43, pp. 1233-1242, 1996.

[10] R. S. Muller, T. I. Kamins, M. Chan, and P. K. Ko, "Device electronics for integrated circuits," 1986.

[11] P. V. Gray and D. M. Brown, "Density of SiO2–Si interface states," *Applied Physics Letters,* vol. 8, pp. 31-33, 1966.

[12] J. Maserjian and N. Zamani, "Behavior of the Si/SiO2 interface observed by Fowler‐Nordheim tunneling," *Journal of Applied Physics,* vol. 53, pp. 559-567, 1982.

[13] Z. Chen, P.-L. Ong, Y. Wang, and L. Han, "Lateral heating of SiO2/Si: Interfacial Si structure change causing tunneling current reduction," *Applied Physics Letters,* vol. 100, p. 171602, 2012.

[14] J. Fitch, C. Bjorkman, G. Lucovsky, F. Pollak, and X. Yin, "Intrinsic stress and stress gradients at the SiO2/Si interface in structures prepared by thermal oxidation of Si and subjected to rapid thermal annealing," *Journal of Vacuum Science & Technology B,* vol. 7, pp. 775-781, 1989.

[15] R. Jaccodine and W. Schlegel, "Measurement of Strains at Si‐SiO2 Interface," *Journal of Applied Physics,* vol. 37, pp. 2429-2434, 1966.

[16] E. H. Nicollian, J. R. Brews, and E. H. Nicollian, *MOS (metal oxide semiconductor) physics and technology* vol. 1987: Wiley New York et al., 1982.

[17] K. Nakajima, M. Suzuki, K. Kimura, M. Yamamoto, A. Teramoto, T. Ohmi*, et al.*, "Lattice distortion at SiO2/Si (001) interface studied with high-resolution Rutherford

backscattering spectroscopy/channeling," *Japanese journal of applied physics,* vol. 45, p. 2467, 2006.
[18] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE,* vol. 91, pp. 305-327, 2003.
[19] A. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultra-thin gate dielectrics," *Journal of applied physics,* vol. 81, pp. 7900-7908, 1997.
[20] M. Lenzlinger and E. Snow, "Fowler‐Nordheim Tunneling into Thermally Grown SiO2," *Journal of Applied physics,* vol. 40, pp. 278-283, 1969.
[21] K. F. Schuegraf and C. Hu, "Hole injection SiO 2 breakdown model for very low voltage lifetime extrapolation," *Electron Devices, IEEE Transactions on,* vol. 41, pp. 761-767, 1994.
[22] S. K. Gupta, J. Akhtar, and J. Singh, *Materials and Processing for Gate Dielectrics on Silicon Carbide (SiC) Surface*: INTECH Open Access Publisher, 2012.
[23] P.-L. Ong, Z. Chen, A. Haggag, and T.-Y. Luo, "Large leakage-current reduction of ultrathin industrial SiON wafers induced by phonon-energy-coupling enhancement," *Electrochemical and Solid-State Letters,* vol. 11, pp. H293-H295, 2008.

Chapter 4

[1] T. Hou, J. Gutt, C. Lim, S. Marcus, C. Pomarede, M. Gardner*, et al.*, "Improved scalability of high-k gate dielectrics by using Hf-aluminates," in *Electrochemical Society Meeting*, 2002.
[2] S. M. Sze and S. M. Sze, *VLSI technology* vol. 2: McGraw-Hill New York, 1988.
[3] H. Leplan, B. Geenen, J.-Y. Robic, and Y. Pauleau, "Residual stresses in silicon dioxide thin films prepared by reactive electron beam evaporation," in *1994 International Symposium on Optical Interference Coatings*, 1994, pp. 1263-1274.
[4] R. Ishihara, Y. Hiroshima, D. Abe, B. D. Van Dijk, P. C. Van Der Wilt, S. Higashi*, et al.*, "Single-grain Si TFTs with ECR-PECVD gate SiO< sub> 2</sub>," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 500-502, 2004.
[5] H. Bartzsch, D. Glöß, B. Böcher, P. Frach, and K. Goedicke, "Properties of SiO2 and Al2O3 films for electrical insulation applications deposited by reactive pulse magnetron sputtering," *Surface & coatings technology,* vol. 174, pp. 774-778, 2003.
[6] M. Ritala and M. Leskela, "Atomic layer deposition," vol. 1, ed: Academic Press: San Diego, CA, 2001, p. 103.
[7] M. Leskelä and M. Ritala, "Atomic layer deposition (ALD): from precursors to thin film structures," *Thin solid films,* vol. 409, pp. 138-146, 2002.
[8] S. M. George, "Atomic layer deposition: an overview," *Polymer,* vol. 1550, p. 125, 2010.
[9] J. Ferguson, E. Smith, A. Weimer, and S. George, "ALD of SiO2 at Room Temperature Using TEOS and H 2 O with NH 3 as the Catalyst," *Journal of The Electrochemical Society,* vol. 151, pp. G528-G535, 2004.
[10] J. W. Lim, S. J. Yun, and J. H. Lee, "Low-temperature growth of SiO 2 films by plasma-enhanced atomic layer deposition," *ETRI journal,* vol. 27, pp. 118-121, 2005.
[11] B. Burton, S. Kang, S. Rhee, and S. George, "SiO2 Atomic Layer Deposition Using Tris (dimethylamino) silane and Hydrogen Peroxide Studied by in Situ Transmission FTIR Spectroscopy," *The Journal of Physical Chemistry C,* vol. 113, pp. 8249-8257, 2009.
[12] J. K. Kang and C. B. Musgrave, "Mechanism of atomic layer deposition of SiO 2 on the silicon (100)-2× 1 surface using SiCl 4 and H 2 O as precursors," *Journal of Applied Physics,* vol. 91, pp. 3408-3414, 2002.

[13] M. L. O'Neill, H. R. Bowen, A. Derecskei-Kovacs, K. S. Cuthill, B. Han, and M. Xiao, "Impact of Aminosilane Precursor Structure on Silicon Oxides by Atomic Layer Deposition," *Interface-Electrochemical Society,* vol. 20, p. 33, 2011.

[14] J. Li, J. Wu, C. Zhou, B. Han, E. J. Karwacki, M. Xiao*, et al.*, "On the Dissociative Chemisorption of Tris(dimethylamino)silane on Hydroxylated SiO2(001) Surface," *The Journal of Physical Chemistry C,* vol. 113, pp. 9731-9736, 2009/06/04 2009.

[15] Y. Kinoshita, F. Hirose, H. Miya, K. Hirahara, Y. Kimura, and M. Niwano, "Infrared study of tris(dimethylamino)silane adsorption and ozone irradiation on Si(100) surfaces for ALD of SiO2," *Electrochemical and Solid State Letters,* vol. 10, pp. G80-G83, 2007.

[16] S. Kamiyama, T. Miura, and Y. Nara, "Comparison between SiO< sub> 2</sub> films deposited by atomic layer deposition with SiH< sub> 2</sub>[N (CH< sub> 3</sub>)< sub> 2</sub>]< sub> 2</sub> and SiH [N (CH< sub> 3</sub>)< sub> 2</sub>]< sub> 3</sub> precursors," *Thin solid films,* vol. 515, pp. 1517-1521, 2006.

[17] J. Bachmann, R. Zierold, Y. T. Chong, R. Hauert, C. Sturm, R. Schmidt-Grund*, et al.*, "A Practical, Self-Catalytic, Atomic Layer Deposition of Silicon Dioxide," *Angewandte Chemie International Edition,* vol. 47, pp. 6177-6179, 2008.

[18] D. Hiller, R. Zierold, J. Bachmann, M. Alexe, Y. Yang, J. W. Gerlach*, et al.*, "Low temperature silicon dioxide by thermal atomic layer deposition: Investigation of material properties," *Journal of Applied Physics,* vol. 107, pp. 064314-064314-10, 2010.

[19] F. Hirose, Y. Kinoshita, S. Shibuya, Y. Narita, H. Miya, K. Hirahara*, et al.*, "Low-temperature-atomic-layer-deposition of SiO2 with Tris (dimethylamino) Silane (TDMAS) and Ozone using Temperature Controlled Water Vapor Treatment," *ECS Transactions,* vol. 19, pp. 417-426, 2009.

[20] G. Liu, R. Bhatia, E. W. Deguns, M. J. Dalberth, M. J. Sowa, A. Bertuch*, et al.*, "High rate growth of SiO_2 by thermal ALD using tris(dimethylamino)silane and ozone," in *11th International Conference on Atomic Layer Deposition*, Cambridge, MA, USA, 2011.

[21] S. Li, L. Han, and Z. Chen, "The interfacial quality of HfO2 on silicon with different thicknesses of the chemical oxide interfacial layer," *Journal of The Electrochemical Society,* vol. 157, pp. G221-G224, 2010.

[22] Z. Chen, P.-L. Ong, Y. Wang, and L. Han, "Lateral heating of SiO< inf> 2</inf>/Si: Interfacial Si structure change causing tunneling current reduction," *Applied Physics Letters,* vol. 100, pp. 171602-171602-4, 2012.

[23] J. C. Hackley, T. Gougousi, and J. D. Demaree, "Nucleation of< equation>< font face='verdana'> HfO< sub> 2</sub></equation> atomic layer deposition films on chemical oxide and H-terminated Si," *Journal of Applied Physics,* vol. 102, pp. 034101-034101-7, 2007.

[24] M. T. Ho, Y. Wang, R. T. Brewer, L. S. Wielunski, Y. J. Chabal, N. Moumen*, et al.*, "In situ infrared spectroscopy of hafnium oxide growth on hydrogen-terminated silicon surfaces by atomic layer deposition," *Applied Physics Letters,* vol. 87, pp. 133103-133103-3, 2005.

[25] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE,* vol. 91, pp. 305-327, 2003.

[26] S.-H. Lo, D. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *Electron Device Letters, IEEE,* vol. 18, pp. 209-211, 1997.

[27] B. Brar, G. Wilk, and A. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin SiO< inf> 2</inf>," *Applied Physics Letters,* vol. 69, pp. 2728-2730, 1996.

[28] H. Sasaki, M. Ono, T. Yoshitomi, T. Ohguro, S.-I. Nakamura, M. Saito*, et al.*, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 43, pp. 1233-1242, 1996.

[29] M. Bjork, J. Knoch, H. Schmid, H. Riel, and W. Riess, "Silicon nanowire tunneling field-effect transistors," *Applied Physics Letters,* vol. 92, pp. 193504-193504-3, 2008.

[30] R. S. Muller, T. I. Kamins, M. Chan, and P. K. Ko, *Device electronics for integrated circuits*, 1986.

[31] C. Osburn and D. Ormond, "Dielectric breakdown in silicon dioxide films on silicon I. Measurement and interpretation," *Journal of The Electrochemical Society,* vol. 119, pp. 591-597, 1972.

[32] K. Yamabe, K. Taniguchi, and Y. Matsushita, "Thickness dependence of dielectric breakdown failure of thermal SiO2 films," in *Reliability Physics Symposium, 1983. 21st Annual*, 1983, pp. 184-190.

[33] C. Osburn and E. Weitzman, "Electrical conduction and dielectric breakdown in silicon dioxide films on silicon," *Journal of The Electrochemical Society,* vol. 119, pp. 603-609, 1972.

[34] W. J. Patrick, G. C. Schwartz, J. D. Chapple‐Sokol, R. Carruthers, and K. Olsen, "Plasma‐Enhanced Chemical Vapor Deposition of Silicon Dioxide Films Using Tetraethoxysilane and Oxygen: Characterization and Properties of Films," *Journal of The Electrochemical Society,* vol. 139, pp. 2604-2613, 1992.

[35] S. Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, and M. Umeno, "Investigations of SiO 2/n-GaN and Si 3 N 4/n-GaN insulator–semiconductor interfaces with low interface state density," *Applied Physics Letters,* vol. 73, pp. 809-811, 1998.

[36] S. E. Alexandrov, N. McSporran, and M. L. Hitchman, "Remote AP‐PECVD of Silicon Dioxide Films from Hexamethyldisiloxane (HMDSO)," *Chemical Vapor Deposition,* vol. 11, pp. 481-490, 2005.

Chapter 5

[1] S. Li, L. Han, and Z. Chen, "The interfacial quality of HfO2 on silicon with different thicknesses of the chemical oxide interfacial layer," *Journal of The Electrochemical Society,* vol. 157, pp. G221-G224, 2010.

[2] Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng*, et al.*, "AlGaN/GaN MOS-HEMT With Dielectric and Interfacial Passivation Layer Grown by Atomic Layer Deposition," *Electron Device Letters, IEEE,* vol. 29, pp. 838-840, 2008.

[3] E. Bersch, S. Rangan, R. A. Bartynski, E. Garfunkel, and E. Vescovo, "Band offsets of ultrathin high-κ oxide films with Si," *Physical Review B,* vol. 78, p. 085114, 2008.

[4] H. Kim, P. C. McIntyre, and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO2 dielectrics grown by atomic layer deposition," *Applied physics letters,* vol. 82, pp. 106-108, 2003.

[5] Y. J. Cho, N. Nguyen, C. Richter, J. Ehrstein, B. H. Lee, and J. C. Lee, "Spectroscopic ellipsometry characterization of high-k dielectric HfO2 thin films and the high-temperature annealing effects on their optical properties," *Applied physics letters,* vol. 80, pp. 1249-1251, 2002.

[6] M.-Y. Ho, H. Gong, G. Wilk, B. Busch, M. Green, P. Voyles*, et al.*, "Morphology and crystallization kinetics in HfO2 thin films grown by atomic layer deposition," *Journal of Applied Physics,* vol. 93, pp. 1477-1481, 2003.

[7] Y.-S. Lin, R. Puthenkovilakam, and J. Chang, "Dielectric property and thermal stability of HfO2 on silicon," *Applied physics letters,* vol. 81, pp. 2041-2043, 2002.

[8] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank*, et al.*, "Extremely scaled gate-first high-k/metal gate stack with EOT of 0.55 nm using novel interfacial layer scavenging techniques for 22nm technology node and beyond," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 138-139.

[9] T. Ando, M. Frank, K. Choi, C. Choi, J. Bruley, M. Hopstaken*, et al.*, "Understanding mobility mechanisms in extremely scaled HfO 2 (EOT 0.42 nm) using remote interfacial layer scavenging technique and V t-tuning dipoles with gate-first process," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.

[10] C. Choi, C. Y. Kang, S. J. Rhee, M. S. Abkar, S. A. Krishna, M. Zhang*, et al.*, "Fabrication of TaN-gated ultra-thin MOSFETs (EOT< 1.0 nm) with HfO/sub 2/using a novel oxygen scavenging process for sub 65 nm application," in *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, 2005, pp. 226-227.

[11] M. Takahashi, A. Ogawa, A. Hirano, Y. Kamimuta, Y. Watanabe, K. Iwamoto*, et al.*, "Gate-First Processed FUSI/HfO 2/HfSiO x/Si MOSFETs with EOT= 0.5 nm-Interfacial Layer Formation by Cycle-by-Cycle Deposition and Annealing," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 523-526.

[12] J. Huang, D. Heh, P. Sivasubramani, P. Kirsch, G. Bersuker, D. Gilmer*, et al.*, "Gate first high-k/metal gate stacks with zero SiO x interface achieving EOT= 0.59 nm for 16nm application," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 34-35.

[13] E. Gusev, C. Cabral Jr, M. Copel, C. D'Emic, and M. Gribelyuk, "Ultrathin HfO< sub> 2</sub> films grown on silicon by atomic layer deposition for advanced gate dielectrics applications," *Microelectronic Engineering,* vol. 69, pp. 145-151, 2003.

[14] Y. Morita, A. Hirano, S. Migita, H. Ota, T. Nabatame, and A. Toriumi, "Impact of Surface Hydrophilicization prior to Atomic Layer Deposition for HfO2/Si Direct-Contact Gate Stacks," *Applied physics express,* vol. 2, p. 011201, 2009.

[15] J. C. Hackley, J. D. Demaree, and T. Gougousi, "Growth and interface of HfO2 films on H-terminated Si from a TDMAH and H2O atomic layer deposition process," *Journal of Vacuum Science & Technology A,* vol. 26, pp. 1235-1240, 2008.

[16] K. Li, S. Li, N. Li, D. A. Dixon, and T. M. Klein, "Tetrakis (dimethylamido) hafnium adsorption and reaction on hydrogen terminated Si (100) surfaces," *The Journal of Physical Chemistry C,* vol. 114, pp. 14061-14075, 2010.

[17] W. Tsai, R. Carter, H. Nohira, M. Caymax, T. Conard, V. Cosnier*, et al.*, "Surface preparation and interfacial stability of high-k dielectrics deposited by atomic layer chemical vapor deposition," *Microelectronic Engineering,* vol. 65, pp. 259-272, 2003.

[18] J. C. Hackley, T. Gougousi, and J. D. Demaree, "Nucleation of< equation>< font face='verdana'> HfO< sub> 2</sub></equation> atomic layer deposition films on chemical oxide and H-terminated Si," *Journal of Applied Physics,* vol. 102, pp. 034101-034101-7, 2007.

[19] M. Copel, M. Gribelyuk, and E. Gusev, "Structure and stability of ultrathin zirconium oxide layers on Si (001)," *Applied Physics Letters,* vol. 76, pp. 436-438, 2000.

[20] E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha*, et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 20.1. 1-20.1. 4.

[21] S. Guha, E. Gusev, H. Okorn-Schmidt, M. Copel, L.-A. Ragnarsson, N. Bojarczuk*, et al.*, "High temperature stability of Al 2 O 3 dielectrics on Si: Interfacial metal diffusion and mobility degradation," *Applied Physics Letters,* vol. 81, pp. 2956-2958, 2002.

[22] R. L. Puurunen, W. Vandervorst, W. F. Besling, O. Richard, H. Bender, T. Conard*, et al.*, "Island growth in the atomic layer deposition of zirconium oxide and aluminum oxide on hydrogen-terminated silicon: Growth mode modeling and transmission electron microscopy," *Journal of applied physics,* vol. 96, pp. 4878-4889, 2004.

[23] P. Kirsch, M. Quevedo-Lopez, H.-J. Li, Y. Senzaki, J. Peterson, S. Song*, et al.*, "Nucleation and growth study of atomic layer deposited HfO2 gate dielectrics resulting in improved scaling and electron mobility," *Journal of applied physics,* vol. 99, p. 023508, 2006.

[24] R. Methaapanon and S. F. Bent, "Comparative Study of Titanium Dioxide Atomic Layer Deposition on Silicon Dioxide and Hydrogen-Terminated Silicon," *The Journal of Physical Chemistry C,* vol. 114, pp. 10498-10504, 2010.

[25] M. Copel, E. Cartier, E. Gusev, S. Guha, N. Bojarczuk, and M. Poppeller, "Robustness of ultrathin aluminum oxide dielectrics on Si (001)," *Applied Physics Letters,* vol. 78, pp. 2670-2672, 2001.

[26] E. Gusev, M. Copel, E. Cartier, I. Baumvol, C. Krug, and M. Gribelyuk, "High-resolution depth profiling in ultrathin Al2O3 films on Si," *Applied Physics Letters,* vol. 76, pp. 176-178, 2000.

[27] M.-T. Ho, Y. Wang, R. Brewer, L. Wielunski, Y. Chabal, N. Moumen*, et al.*, "In situ infrared spectroscopy of hafnium oxide growth on hydrogen-terminated silicon surfaces by atomic layer deposition," *Applied Physics Letters,* vol. 87, pp. 133103-133103-3, 2005.

[28] M. Yang, E. P. Gusev, M. Ieong, O. Gluschenkov, D. C. Boyd, K. K. Chan*, et al.*, "Performance dependence of CMOS on silicon substrate orientation for ultrathin oxynitride and HfO 2 gate dielectrics," *Electron Device Letters, IEEE,* vol. 24, pp. 339-341, 2003.

[29] E. Gusev, H. Shang, M. Copel, M. Gribelyuk, C. DEmic, P. Kozlowski*, et al.*, "Microstructure and thermal stability of HfO 2 gate dielectric deposited on Ge (100)," *Applied physics letters,* vol. 85, pp. 2334-2336, 2004.

[30] A. Delabie, R. L. Puurunen, B. Brijs, M. Caymax, T. Conard, B. Onsia*, et al.*, "Atomic layer deposition of hafnium oxide on germanium substrates," *Journal of applied physics,* vol. 97, p. 064104, 2005.

[31] M. Green, M.-Y. Ho, B. Busch, G. Wilk, T. Sorsch, T. Conard*, et al.*, "Nucleation and growth of atomic layer deposited HfO 2 gate dielectric layers on chemical oxide (Si–O–H) and thermal oxide (SiO 2 or Si–O–N) underlayers," *Journal of Applied Physics,* vol. 92, pp. 7168-7174, 2002.

[32] S. Monaghan, J. Greer, and S. Elliott, "Atomic scale model interfaces between high-k hafnium silicates and silicon," *Physical Review B,* vol. 75, p. 245304, 2007.

[33] B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters,* vol. 76, pp. 1926-1928, 2000.

[34] C. B. Samantaray and Z. Chen, "Reduction of gate leakage current of HfSiON dielectrics through enhanced phonon-energy coupling," *Applied physics letters,* vol. 89, p. 162903, 2006.

Chapter 6

[1] K. Kukli, J. Aarik, A. Aidla, H. Siimon, M. Ritala, and M. Leskelä, "In situ study of atomic layer epitaxy growth of tantalum oxide thin films from Ta (OC< sub> 2</sub> H< sub> 5</sub>)< sub> 5</sub> and H< sub> 2</sub> O," *Applied surface science,* vol. 112, pp. 236-242, 1997.

[2] R. L. Puurunen, "Analysis of hydroxyl group controlled atomic layer deposition of hafnium dioxide from hafnium tetrachloride and water," *Journal of applied physics,* vol. 95, pp. 4777-4786, 2004.

[3] R. L. Puurunen, "Correlation between the growth-per-cycle and the surface hydroxyl group concentration in the atomic layer deposition of aluminum oxide from trimethylaluminum and water," *Applied surface science,* vol. 245, pp. 6-10, 2005.

[4] Y. Morita, A. Hirano, S. Migita, H. Ota, T. Nabatame, and A. Toriumi, "Impact of Surface Hydrophilicization prior to Atomic Layer Deposition for HfO2/Si Direct-Contact Gate Stacks," *Applied physics express,* vol. 2, p. 011201, 2009.

[5] J. C. Hackley, T. Gougousi, and J. D. Demaree, "Nucleation of HfO2 atomic layer deposition films on chemical oxide and H-terminated Si," *Journal of Applied Physics,* vol. 102, p. 034101, 2007.

[6] J. Molina, C. Zuniga, W. Calleja, P. Rosales, A. Torres, and A. Herrera-Gomez, "Physical and electrical characteristics of atomic-layer deposition-HfO2 films deposited on Si substrates having different silanol Si-OH densities," *Journal of Vacuum Science & Technology A,* vol. 31, p. 01A132, 2013.

[7] J. Molina, C. Zuniga, W. Calleja, P. Rosales, A. Torres, and A. Herrera-Gomez, "Physical and electrical characteristics of atomic-layer deposition-HfO2 films deposited on Si substrates having different silanol Si-OH densities," *Journal of Vacuum Science & Technology A,* vol. 31, p. 01A132, 2012.

[8] M. Green, M.-Y. Ho, B. Busch, G. Wilk, T. Sorsch, T. Conard*, et al.*, "Nucleation and growth of atomic layer deposited HfO2 gate dielectric layers on chemical oxide (Si–O–H) and thermal oxide (SiO2 or Si–O–N) underlayers," *Journal of Applied Physics,* vol. 92, pp. 7168-7174, 2002.

[9] W. Tsai, L.-A. Ragnarsson, L. Pantisano, P. Chen, B. Onsia, T. Schram*, et al.*, "Performance comparison of sub 1 nm sputtered TiN/HfO/sub 2/nMOS and pMOSFETs," in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, 2003, pp. 13.2. 1-13.2. 4.

[10] A. Delabie, R. L. Puurunen, B. Brijs, M. Caymax, T. Conard, B. Onsia*, et al.*, "Atomic layer deposition of hafnium oxide on germanium substrates," *Journal of applied physics,* vol. 97, p. 064104, 2005.

[11] S. Li, L. Han, and Z. Chen, "The interfacial quality of HfO2 on silicon with different thicknesses of the chemical oxide interfacial layer," *Journal of The Electrochemical Society,* vol. 157, pp. G221-G224, 2010.

[12] S. Ichimura, A. Kurokawa, K. Nakamura, H. Itoh, H. Nonaka, and K. Koike, "Ultrathin SiO< sub> 2</sub> film growth on Si by highly concentrated ozone," *Thin Solid Films,* vol. 377, pp. 518-524, 2000.

[13] J. F. Moulder, W. F. Stickle, P. E. Sobol, and K. D. Bomben, *Handbook of X-ray photoelectron spectroscopy* vol. 40: Perkin Elmer Eden Prairie, MN, 1992.

[14] E. McCafferty and J. Wightman, "Determination of the concentration of surface hydroxyl groups on metal oxide films by a quantitative XPS method," *Surface and Interface Analysis,* vol. 26, pp. 549-564, 1998.

[15] B. Brar, G. Wilk, and A. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin SiO2," *Applied physics letters,* vol. 69, pp. 2728-2730, 1996.

[16] B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters,* vol. 76, pp. 1926-1928, 2000.

[17] E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha*, et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 20.1. 1-20.1. 4.

[18] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros*, et al.*, "High-frequency response of 100 nm integrated CMOS transistors with high-K gate dielectrics," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 10.6. 1-10.6. 4.

[19] D. W. Barlage, J. T. O'Keeffe, J. T. Kavalieros, M. M. Nguyen, and R. S. Chau, "Inversion MOS capacitance extraction for high-leakage dielectrics using a transmission line equivalent circuit," *Electron Device Letters, IEEE,* vol. 21, pp. 454-456, 2000.

[20] J. D. Wiley and G. Miller, "Series resistance effects in semiconductor CV profiling," *Electron Devices, IEEE Transactions on,* vol. 22, pp. 265-272, 1975.

Chapter 7

[1] M. Green, M.-Y. Ho, B. Busch, G. Wilk, T. Sorsch, T. Conard*, et al.*, "Nucleation and growth of atomic layer deposited HfO 2 gate dielectric layers on chemical oxide (Si–O–H) and thermal oxide (SiO 2 or Si–O–N) underlayers," *Journal of Applied Physics,* vol. 92, pp. 7168-7174, 2002.

[2] J. C. Hackley, T. Gougousi, and J. D. Demaree, "Nucleation of< equation>< font face='verdana'> HfO< sub> 2</sub></equation> atomic layer deposition films on chemical oxide and H-terminated Si," *Journal of Applied Physics,* vol. 102, pp. 034101-034101-7, 2007.

[3] W. Tsai, R. Carter, H. Nohira, M. Caymax, T. Conard, V. Cosnier*, et al.*, "Surface preparation and interfacial stability of high-k dielectrics deposited by atomic layer chemical vapor deposition," *Microelectronic Engineering,* vol. 65, pp. 259-272, 2003.

[4] F. De Smedt, G. Stevens, S. De Gendt, I. Cornelissen, S. Arnauts, M. Meuris*, et al.*, "A wet chemical method for the determination of thickness of SiO2 layers below the nanometer level," *Journal of The Electrochemical Society,* vol. 146, pp. 1873-1878, 1999.

[5] F. De Smedt, C. Vinckier, I. Cornelissen, S. De Gendt, and M. Heyns, "A detailed study on the growth of thin oxide layers on silicon using ozonated solutions," *Journal of the Electrochemical Society,* vol. 147, pp. 1124-1129, 2000.

[6] W. Tsai, L.-A. Ragnarsson, L. Pantisano, P. Chen, B. Onsia, T. Schram*, et al.*, "Performance comparison of sub 1 nm sputtered TiN/HfO< sub> 2</sub> nMOS and pMOSFETs," in *Electron Devices Meeting, 2003. IEDM'03 Technical Digest. IEEE International*, 2003, pp. 13.2. 1-13.2. 4.

[7] G. Gould and E. Irene, "An in situ study of aqueous HF treatment of silicon by contact angle measurement and ellipsometry," *Journal of The Electrochemical Society,* vol. 135, pp. 1535-1539, 1988.

[8] S. Li, L. Han, and Z. Chen, "The interfacial quality of HfO2 on silicon with different thicknesses of the chemical oxide interfacial layer," *Journal of The Electrochemical Society,* vol. 157, pp. G221-G224, 2010.

[9] J. S. Judge, "A study of the dissolution of SiO2 in acidic fluoride solutions," *Journal of The Electrochemical Society,* vol. 118, pp. 1772-1775, 1971.

[10] K. R. Williams and R. S. Muller, "Etch rates for micromachining processing," *Microelectromechanical Systems, Journal of,* vol. 5, pp. 256-269, 1996.

[11] B. Brar, G. Wilk, and A. Seabaugh, "Direct extraction of the electron tunneling effective mass in ultrathin SiO< inf> 2</inf>," *Applied Physics Letters,* vol. 69, pp. 2728-2730, 1996.

[12] E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha*, et al.*, "Ultrathin high-K gate stacks for advanced CMOS devices," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 20.1. 1-20.1. 4.

[13] B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters,* vol. 76, pp. 1926-1928, 2000.

[14] D. Barlage, R. Arghavani, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros*, et al.*, "High-frequency response of 100 nm integrated CMOS transistors with high-K gate dielectrics," in *Electron Devices Meeting, 2001. IEDM'01. Technical Digest. International*, 2001, pp. 10.6. 1-10.6. 4.

[15] D. W. Barlage, J. T. O'Keeffe, J. T. Kavalieros, M. M. Nguyen, and R. S. Chau, "Inversion MOS capacitance extraction for high-leakage dielectrics using a transmission line equivalent circuit," *Electron Device Letters, IEEE,* vol. 21, pp. 454-456, 2000.

[16] J. D. Wiley and G. Miller, "Series resistance effects in semiconductor CV profiling," *Electron Devices, IEEE Transactions on,* vol. 22, pp. 265-272, 1975.

Chapter 8

[1] S. I. Association, "International Technology Roadmap for Semiconductors, 2013 edition," 2013.

[2] D. Hiller, R. Zierold, J. Bachmann, M. Alexe, Y. Yang, J. Gerlach*, et al.*, "Low temperature silicon dioxide by thermal atomic layer deposition: Investigation of material properties," *Journal of Applied Physics,* vol. 107, p. 064314, 2010.

Vita

Lei Han was born in Taigu, Shanxi, P. R. China. She received a Bachelor degree of Engineering with Business Management as a minor from Tianjin University, Tianjin, P. R. China in 2007. She began her Ph.D. studies in Electrical Engineering at the University of Kentucky in 2008. She received a Master of Science degree in Electrical Engineering from the University of Kentucky in 2012.

Publications

L. Han, J. Pan, Q. Zhang, S. Li and Z. Chen, “Atomic layer deposition of high quality HfO_2 using in-situ formed hydrophilic oxide as an interfacial layer,” ECS Journal of Solid State Science and Technology (original Journal of The Electrochemical Society), 3 (12), N155, 2014.

L. Han and Z. Chen, “High-quality thin SiO_2 films grown by atomic layer deposition using tris(dimethylamino) silane (TDMAS) and ozone,” ECS Journal of Solid State Science and Technology, 2 (11), N228, 2013.

Z. Chen, P. Ong, Y. Wang, L. Han, “Lateral heating of SiO_2/Si: interfacial Si structure change causing tunneling current reduction,” Applied Physics Letters, 100, 171602, 2012.

S. Li, L. Han and Z. Chen, “The interfacial quality of HfO_2 on silicon with different thicknesses of the chemical oxide interfacial layer,” Journal of The Electrochemical Society, 157, G221, 2010.

L. Han and Z. Chen, "Atomic layer deposition of HfO_2 using HF etched thermal and RTP SiO_2 as in terfacial layers," ECS Transactions, 61(2), 143-149, 2014.

L. Han and Z. Chen, "Ultrathin SiO_2 films grown by atomic layer deposition using tris(dimethylamino) silane (TDMAS) and ozone," ECS Transactions, 58(10), 307-316, 2013.